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Development of piezoresistive cantilevers for applications in quantum twisting microscope experiments

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Abstract

This thesis presents the design, simulation, and fabrication of a piezoresistive cantilever intended for integration into a cryogenic quantum twisting microscope (QTM). Piezoresistive readout offers an attractive alternative to optical detection in low-temperature environments due to its compact form factor and compatibility with standard microfabrication techniques. The cantilever design is based on a double-leg structure. A two-layer architecture consisting of doped silicon and silicon nitride was employed. Finite element simulations were conducted to optimize key geometrical parameters such as leg length, width, and layer thickness, balancing sensitivity and structural integrity. The fabrication process was developed using commercially available silicon-on-insulator (SOI) wafers and standard cleanroom techniques. Emphasis was placed on achieving a simple and reproducible process flow that remains compatible with the constraints of a university-scale facility. Key challenges, including electrode integration and the alignment of front- and backside features, were addressed during process development. Initial measurements confirm the viability of the cantilever design for sensing deflection at room temperature.

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1 Introduction

In recent decades, the ability to probe and manipulate matter at the nanoscale has become central to progress in both fundamental physics and applied nanotechnology. Among the techniques that have enabled such exploration, scanning probe microscopy (SPM) stands out for its versatility and resolution. One of the most widely used SPM techniques is Atomic Force Microscopy (AFM), which provides topographical and mechanical information with atomic-scale resolution [1].

With the emergence of complex quantum materials such as twisted bilayer graphene and other moiré systems, new forms of scanning probe techniques have been developed to explore their electronic properties. One such development is the Quantum Twisting Microscope (QTM) [2]. Recently developed in 2023, QTM is a novel SPM technique that facilitates the measurements of band structures in two-dimensional (2D) materials through electron tunneling spectroscopy. A modified AFM setup is usually employed in the QTM experiments in order to bring the 2D materials together and maintain a stable contact (Fig. 1.1). New exciting results from the QTM have motivated researchers to extend its capability to quantum limit by doing the experiments at cryogenic temperature. In these environments, standard optical detection schemes used in conventional AFMs become less practical due to limited optical access, alignment difficulties, and the heating from light that can disturb low temperature conditions [3].

Piezoresistive cantilevers offer a promising alternative for deflection sensing in such constrained environments. These cantilevers incorporate strain-sensitive resistors directly into their mechanical structure, converting deflection into a change in electrical resistance. Their compact design, compatibility with CMOS fabrication processes, and ability to operate without optical components make them especially attractive for cryogenic applications [4]. Moreover, the readout can be achieved using relatively simple electronic circuits, such as Wheatstone bridges.

However, the development of such piezoresistive cantilevers suitable for use in QTM is not without challenges. Maximizing sensitivity involves careful tuning of the cantilever geometry and materials. In cryogenic conditions, additional factors such as dopant freeze-out, and the behavior of piezoresistive coefficients at low temperatures must also be considered [4].

The goal of this thesis is to design a prototype piezoresistive cantilever optimized for use in low temperature QTM experiments. In addition to the numerical modeling and simulation of the sensor behavior, a major focus of this work is the fabrication of the cantilever and addressing the experimental challenges associated with it.

The remainder of this thesis is structured as follows: Chapter 2 provides theoretical background on the piezoresistive effect, the mechanical and electrical modeling of piezoresistive cantilevers. Chapter 3 details the COMSOL simulation setup and parametric studies. Chapter 4 discusses the fabrication of the cantilevers, including the characterization and some preliminary tests. Finally, Chapter 5 summarizes the findings and outlines directions for future work.

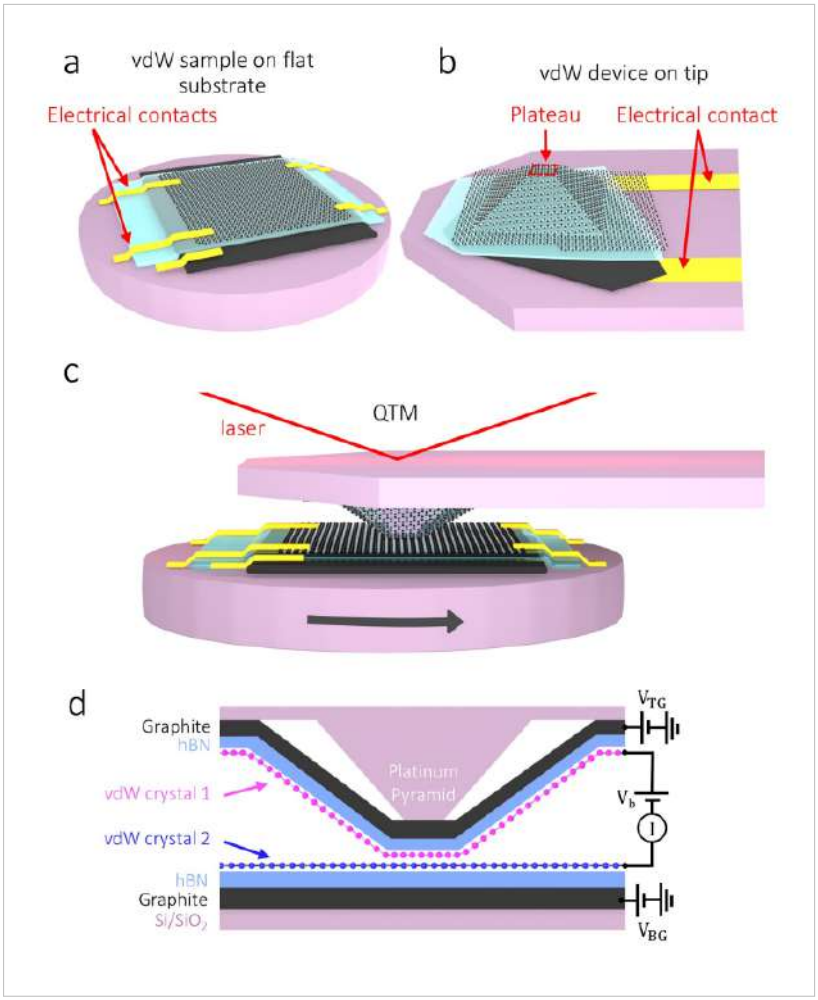


Figure 1.1: (**a**) Sample device is a van-der-Waals (vdW) heterostructure assembled on a flat substrate with electrical contacts. (**b**) Tip device consists of a vdW heterostructure assembled on a AFM cantilever's tip with a flat plateau. (**c**) Tip and sample devices are brought into contact using an AFM and the relative angle between them is controlled with a rotator. (**d**) A voltage bias V_b is applied between the two active vdW layers and the corresponding current I is measured. Adapted from [2]

2 Self-sensing cantilever based on piezoresistive effect

Having motivated the development of a self-sensing cantilever for low-temperature QTM, we now introduce the basic theory behind cantilevers with integrated piezoresistive readout in this chapter. First, it is described how electrical resistance of conductive materials changes when subjected to a mechanical strain, and thus give rise to piezoresistive effect. Following that, we dive deeper into the piezoresistivity of semiconductors particularly in crystalline silicon. Next, the working principle of a cantilever with integrated piezoresistive readout, for detection of the interactions between cantilever tip and sample, is introduced. Finally, the main noise sources in piezoresistive cantilevers that can affect the sensitivity are briefly introduced.

2.1 Piezoresistivity

Pieozoresitive effect is the change in the electrical resistance of a solid when a mechanical stress is applied. The phenomenon was first discovered by William Thomson (Lord Kelvin) in iron and nickel in 1857 [5] and afterwards have been studied systematically in many metals by others [6]. But it have been until 1954 that researchers discovered a much larger piezoresistive effect in silicon and germanium [7]. Since then, they are used widely in commercial pressure sensors and accelerometers.

2.1.1 Fundamentals of piezoresistivity

To understand how and why piezoresistive effect occurs, we first start with the familiar equation for the resistance of a homogeneous material with resistivity ρ, length l, and cross-sectional area A [8]:

$$R = \rho \frac{l}{A}. \tag{2.1}$$

The change in resistance ΔR can be derived from Equation 2.1 and expressed in terms of change in resistivity $\Delta\rho$, length Δl and cross-sectional area ΔA as:

$$\Delta R = \frac{\partial \rho}{\partial R}\Delta\rho + \frac{\partial l}{\partial R}\Delta l + \frac{\partial A}{\partial R}\Delta A, \tag{2.2}$$

and hence the relative change in resistance is given by:

$$\frac{\Delta R}{R} = \frac{\Delta\rho}{\rho} + \frac{\Delta l}{l} - \frac{\Delta A}{A}. \tag{2.3}$$

Using the definition of strain ϵ and its relation to the change in cross-sectional area under an uniaxial stress [9]:

$$\frac{\Delta l}{l} = \epsilon, \tag{2.4}$$

$$\frac{\Delta A}{A} = -2\nu\epsilon, \tag{2.5}$$

with ν is the Poisson ratio, one can rewrite Equation 2.3 into:

$$\frac{\Delta R}{R} = \frac{\Delta\rho}{\rho} + \epsilon + 2\epsilon = \frac{\Delta\rho}{\rho} + (1 + 2\nu)\epsilon. \tag{2.6}$$

The strength of piezoresitive effect of a material can be quantified by the gauge factor G, which is defined as [10]:

$$G = \frac{\Delta R/R}{\epsilon} = \frac{\Delta\rho/\rho}{\epsilon} + 1 + 2\nu. \tag{2.7}$$

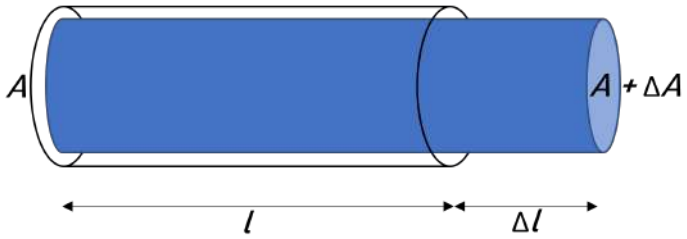


Figure 2.1: Schematic illustration of a solid under a tensile stress

From Equation 2.7 it is apparent that the change in electrical resistance can arise from two main mechanisms: changes in the resistor's dimensions and changes in material resistivity. We know already from mechanical physics that solid will undergo a deformation in the presence of mechanical stresses (Fig. 2.1). Therfore, any conducting material can exhibit piezoresistivity by this geometrical mechanism. This mechanism is responsible for piezoresistive effect in most metals, and the gauge factor depends solely on the mechanical properties of the material. On the other hand, piezorisistivity in semiconductors results primarily from the change in material resistivity while the geometrical contribution to G is negligible. That why the gauge factors of semiconductors are usually up to two orders of magnitude larger than those of metals [10]. The gauge factor of some materials is given in Table 2.1.

2.1.2 Piezoresitivity in doped Silicon

The resistivity ρ of a semiconductor can be expressed as [8]:

Material	Gauge Factor
Cu	1.6
Ni	-12.62
Al	1.4
Pt	2.6
Si(c)	-102 to 135

Table 2.1: Gauge factor of some materials. Adapted from [11].

$$\rho = \frac{1}{\sum_i q_i n_i \mu_i} \tag{2.8}$$

where q_i is the charge of the carrier, n_i is the number of carriers per unit volume, and μ_i is the mobility of the i-th type of carrier. From Equation 2.8, it is clear that any variation in carrier concentration n_i or mobility μ_i directly affects the resistivity of the material. This forms the physical basis of the piezoresistive effect in semiconductors.

Piezoresistivity in n-type Silicon

In n-type silicon, the piezoresistive effect arises from changes in the conduction band structure under applied mechanical stress [12]. Under zero load, the conduction band of silicon consists of six degenerated energy valleys. Considering a crystal direction, these valleys can be categorized into two longitudinal and four transverse valleys depending on the orientation of electron motion with respect to this crystal direction.

When mechanical stress is applied to the crystal, this sixfold degeneracy is lifted. For instance, under compressive stress, the energy of the longitudinal valleys, which aligned parallel to the stress direction, is reduced relative to the transverse valleys. Since electrons tend to occupy states with lower energy, a redistribution of carriers occurs — electrons are transferred from the transverse to the longitudinal valleys [13].

Longitudinal valleys have higher effective mass compared to transverse valleys, which results in a decrease in density-of-states weighted effective mass. According to Equation 2.8, this leads to an increase in resistivity. Therefore, the net result of compressive stress in n-type silicon is an increase in resistivity.

Piezoresistivity in p-type Silicon

The piezoresistive behavior in p-type silicon is more complex due to the nature of its valence band structure [14]. There are two main types of charge carriers: light holes and heavy holes, which differ in their effective masses as the names suggested. In the absence of stress, these bands are degenerate, meaning they have the same energy.

Under mechanical stress, this degeneracy is lifted: compressive stress causes the light-hole band to shift upward in energy relative to the heavy-hole band. This shift leads to a

redistribution of holes between these two bands, altering the hole concentration n and the average hole mobility μ.

Additionally, the shifting of valence band also induces a band anti-crossing, which in turn results in hole states with effective masses significantly different from either original band. This change in the distribution and transport properties of holes under stress alters the material's resistivity.

Anisotropy and Dopant Dependence

It is also important to note that the piezoresistive effect in single-crystal silicon is highly anisotropic [7]. The magnitude and sign of the piezoresistive coefficients depend strongly on the orientation of the applied stress with respect to the crystal axes. For example, the <110> direction typically exhibits higher sensitivity compared to <100>.

Furthermore, the piezoresistive response is also influenced by the doping concentration and dopant species [15]. Higher doping concentrations tend to reduce the magnitude of piezoresistive effect. The choice between p-type or n-type silicon also impacts the effective piezoresistive coefficients as shown in Table 2.2, which must be considered during device design.

Material	π_{11}	π_{12}	π_{44}
n-Si	-102.2	53.4	-13.6
p-Si	6.6	-1.1	138.1

Table 2.2: Piezoresistive coefficients in n- and p-type silicon. Adapted from [15].

2.2 Piezoresistive cantilever

Piezoresistive cantilevers for AFM were first demonstrated by Tortonese [16]. Since this initial development, numerous efforts have been made to enhance the performance, sensitivity, and reliability of piezoresistive cantilevers [17–19]. These cantilevers are particularly advantageous in experimental environments where optical detection methods are impractical or introduce complications. Furthermore, their fabrication is also compatible with CMOS fabrication processes. Now piezoresitive cantilever have been employed in a wide range of application including biosensing [20], chemical detection [21], data storage [22] and the investigation of quantum materials [23].

2.2.1 Piezoresistive readout

The change in resistance of a piezoresistive sensor can be conveniently measured using relatively simple circuits, such as a Wheatstone bridge. This method is well-suited for detecting small resistance changes caused by strain in the piezoresistive elements.

However, semiconductor piezoresistors are also sensitive to environmental variables, especially temperature [10]. Temperature fluctuations and other common-mode noise

sources can induce resistance changes unrelated to mechanical deformation. To mitigate such effects, an unstrained reference piezoresistor is typically placed in close proximity to the active sensor and connected in the same branch of the Wheatstone bridge (Fig. 2.2).

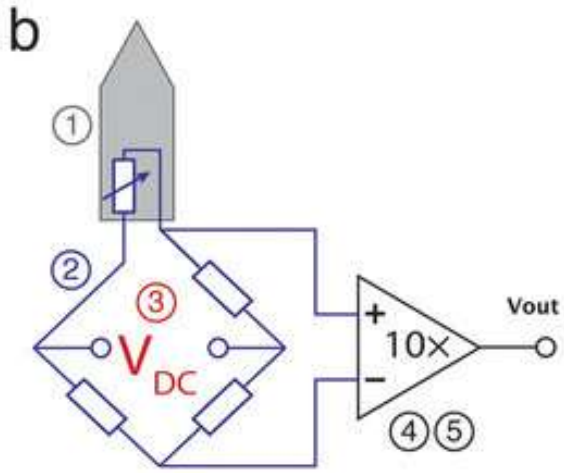


Figure 2.2: Wheatstone bride as read-out circuit for piezoresistive cantilever. Adapted from [24].

The output voltage V_{out} of the Wheatstone bridge depends on the change in resistance ΔR_i of the piezoresistors, which are directly related to the mechanical strain experienced by the cantilever. For a given bias voltage V_{bias}, the general output voltage is:

$$V_{\text{out}} = \frac{\Delta R_1 + \Delta R_3 - \Delta R_2 - \Delta R_4}{R} V_{\text{bias}} \tag{2.9}$$

For a balanced quarter-bridge configuration, where only one of the resistors acts as strain sensor, the equation simplifies to:

$$V_{\text{out}} \approx \frac{1}{4} \frac{\Delta R}{R} V_{\text{bias}} \tag{2.10}$$

As this analysis shows, the output voltage is directly proportional to the relative change in resistance $\Delta R/R$. Therefore, if the piezoresistive coefficients and bias voltage are known, the stress and hence deflection of the cantilever beam can be quantitatively derived from the output voltage of the Wheatstone bridge.

2.2.2 Sensitivity analysis

In the following analysis, we consider a simple cantilever geometry with overall length l_c, width w_c, and thickness t_c. A piezoresistor is placed on the surface of the cantilever and has dimensions l_p, w_p and t_p (Fig. 2.3).

For a point load F applied at the free end of the cantilever, the longitudinal stress at a given position can be described by Euler-Bernoulli beam theory. The local longitudinal stress σ_l at a point (y, z) along the cantilever is given by:

$$\sigma_l = \frac{12(l_c - y)z}{w_c t_c^3} F \tag{2.11}$$

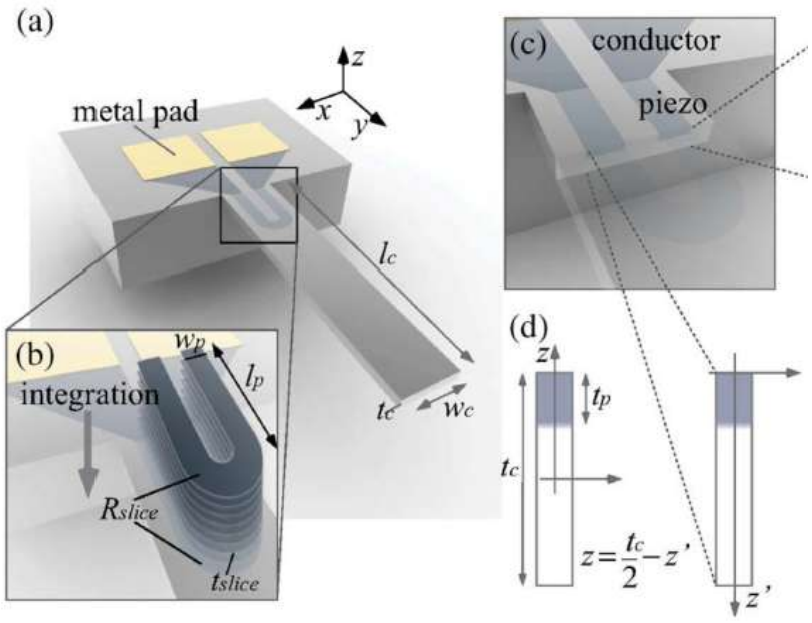


Figure 2.3: Schematic of the cantilever dimensions with integrated piezoresistor. Adapted from [25].

The fractional change in resistivity due to the piezoresistive effect is expressed as:

$$\frac{\Delta\rho}{\rho} = \pi_l \sigma_l + \pi_t \sigma_t \tag{2.12}$$

where π_l and π_t are the piezoresistive coefficients in the longitudinal and transverse directions, respectively, and σ_l, σ_t are the average stresses in those directions. Assuming negligible transverse stresses σ_t and that an infinitesimally thin piezoresistor located at the surface ($z = t_c/2$) with uniform doping across its thickness, the relative change in resistance of the piezoresistor becomes:

$$\begin{aligned} \frac{\Delta R}{R} &= \frac{1}{l_p}\int_0^{l_p} \frac{\Delta\rho}{\rho}\, dy \\ &= \frac{1}{l_p}\int_0^{l_p} \pi_l \frac{12(l_c - y)\frac{t_c}{2}}{w_c t_c^3} F\, dy \\ &= \pi_l \frac{6(l_c - \frac{l_p}{2})}{w_c t_c^2} F \end{aligned} \tag{2.13}$$

Combining Equation 2.13 with the output voltage expression of the Wheatstone bridge, we can derive the theoretical maximum force sensitivity, defined as the ratio of output voltage to applied force:

$$S_{F,\max} = \frac{V_{\text{out}}}{F} = \frac{3\pi_l (l_c - \frac{l_p}{2})}{2 w_c t_c^2} V_{\text{bias}} \tag{2.14}$$

In practice, the actual sensitivity is reduced due to non-idealities in the device geometry and material characteristics. The practical sensitivity can be expressed as:

$$S_F = S_{F,\max}\, \gamma\, \beta^* \tag{2.15}$$

Here, γ is a geometry-dependent factor that accounts for passive resistive regions, e.g. unstrained areas, contact resistances, and interconnects, that contribute to the total resistance but not to the signal. It is defined as:

$$\gamma = \frac{R_{\text{active}}}{R} \tag{2.16}$$

The efficiency factor β^* accounts for the finite thickness and non-uniform doping of the piezoresistor, as well as the variation of the piezoresistive coefficient with dopant concentration. It is given by [16]:

$$\beta^* = \frac{2}{t_c} \frac{\int_{-t_c/2}^{t_c/2} q\mu p(z) P(z) z\, dz}{\int_{-t_c/2}^{t_c/2} q\mu p(z)\, dz} \tag{2.17}$$

In the above expression, $p(z)$ is the dopant concentration profile across the piezoresistor thickness, and $P(z)$ is a piezoresistive factor that captures the dependence of π_l on the local doping level.

2.2.3 Noise sources

Johnson noise

Johnson noise, also known as thermal noise, is a fundamental source of noise present in all resistive elements and represents an intrinsic performance limit for piezoresistive sensors [26]. It originates from the random thermal motion of charge carriers within a conductor, which leads to fluctuations in voltage even in the absence of any applied current or signal.

One of the key characteristics of Johnson noise is that it is both material-independent and frequency-independent over a wide range, which is why it is commonly referred to as "white noise". This means that its power is uniformly distributed across the frequency spectrum.

Under thermal equilibrium, the power spectral density of the voltage fluctuations of Johnson noise depends only on the absolute temperature T and the electrical resistance R of the resistor. The expression for the Johnson noise power spectral density S_J is given by:

$$S_J = 4 k_B T R \tag{2.18}$$

where k_B is the Boltzmann constant. This expression quantifies the amount of noise power per unit bandwidth and is fundamental in determining the minimum detectable signal of piezoresistive cantilevers.

1/f noise

Another significant source of noise in piezoresistive sensors is $1/f$ noise, also referred to as flicker noise. Unlike Johnson noise, $1/f$ noise exhibits a power spectral density that decreases with increasing frequency, following an inverse power law relationship. This characteristic makes it particularly dominant at low frequencies, where it can severely impact the signal-to-noise ratio of the sensor output.

$1/f$ noise arises from fluctuations in the conductance of resistive materials. Although its exact physical origin remains a topic of active research, several mechanisms have been proposed. These include charge carrier trapping and de-trapping at defect sites, variations in the number of mobile charge carriers, and mobility fluctuations within the material.

Unlike Johnson noise, which is a function of the resistance and temperature, $1/f$ noise does not depend directly on the resistance but instead scales with the bias voltage applied across the piezoresistor. A commonly used empirical model to describe $1/f$ noise is the Hooge model [27], which expresses the power spectral density of Hooge noise S_H as:

$$S_H = \frac{\alpha V_{\text{bias}}^2}{N f} \tag{2.19}$$

Here, V_{bias} is the applied bias voltage, N is the total number of free charge carriers in the piezoresistive region, and f is the frequency. The parameter α is the Hooge parameter, a dimensionless quantity that must be determined experimentally and depends on the material properties and fabrication process.

Thermomechanical noise and amplifier noises

In addition to Johnson noise and $1/f$ noise, two other sources of noise that are relevant in piezoresistive cantilevers used in AFM are thermomechanical noise and amplifier noise.

Thermomechanical noise originates from the inherent thermal motion of the cantilever beam itself. It is especially relevant near the resonance frequency of the cantilever. The power spectral density of thermomechanical noise is given by:

$$S_{\text{th}} = \frac{4 k k_b T}{\omega_0 Q} \tag{2.20}$$

where k is the spring constant of the cantilever, k_b is the Boltzmann constant, T is the absolute temperature, ω_0 is the angular resonance frequency of the cantilever, and Q is its quality factor. In most practical applications, thermomechanical noise is smaller than either Johnson noise or $1/f$ noise except near resonance, where it can become dominant.

Amplifier noise, on the other hand, originates from the electronic readout system and is not intrinsically tied to the cantilever structure itself. It depends on the characteristics of the readout circuits.

In practice, these noise sources are typically less significant in comparison to Johnson and $1/f$ noise under standard operating conditions. They are briefly mentioned here for completeness and for consideration in design the piezoresistive cantilevers.

3 Finite element method simulation

To optimize piezoresistive cantilevers for high sensitivity in contact sensing applications, it is essential to understand the influence of key design parameters. Finite Element Method (FEM) simulations were employed to model the mechanical and electrical behavior of the cantilever structures, providing insights into stress distribution and sensitivity under applied loads.

3.1 Modeling of piezoresistivity in FEM

The principle of the FEM is to divide the geometry into a collection of small subdomains, so-called finite elements, and to numerically solve the governing equations over each element. This allows the approximation of complex behaviors within arbitrarily shaped geometries. In the following, bold symbols denote quantities in matrix or tensor form.

3.1.1 Mechanical Modeling

In the mechanical simulation, the stress tensor σ is calculated based on Newton's second law. For a stationary case and assuming linear elastic behavior, which is generally valid for small displacements, COMSOL solves the equation:

$$\nabla \cdot \sigma + \boldsymbol{F}_V = 0 \tag{3.1}$$

Here, $\boldsymbol{F}_V$ represents the body force per unit deformed volume, which can be defined based on boundary conditions.

3.1.2 Electrical Modeling and Piezoresistivity

The electric field $\boldsymbol{E}$ in the piezoresistor is related to the current density $\boldsymbol{J}$ through the total resistivity, including the change in resistivity due to mechanical stress:

$$\boldsymbol{E} = \rho \cdot \boldsymbol{J} + \Delta\rho \cdot \boldsymbol{J} \tag{3.2}$$

Both ρ and $\Delta\rho$ are rank-2 tensors in this context.

COMSOL assumes isotropic conductivity for doped silicon, and the base resistivity ρ is calculated using an empirical fit based on experimental data:

$$\rho_{ij} = \rho = \frac{\sqrt{1 + \frac{n}{n/S + n_{\text{ref}}}}}{qn\mu_0} \tag{3.3}$$

with $\mu_0 = 480\,\text{cm}^2/\text{V/s}$, $n_{\text{ref}} = 4 \times 10^6\,\text{cm}^{-3}$, and $S = 81$ for p-type silicon.

The change in resistivity due to stress is given by:

$$\Delta\rho = \rho\pi \cdot \sigma \tag{3.4}$$

Note that in COMSOL the definition of piezoresistivity tensor π includes the ρ in each element of the tensor. But since we have isotropic resistivity in p-Si and for reasons of clarity it is written in equation 3.4 as a scalar multiple outside of π. π is technically a rank-4 tensor, but for computational purposes it is often expressed in matrix form using Voigt notation, which reduces both the stress and resistivity tensors to 6-element vectors:

$$\begin{bmatrix} \Delta\rho_{xx} \\ \Delta\rho_{yy} \\ \Delta\rho_{zz} \\ \Delta\rho_{yz} \\ \Delta\rho_{xz} \\ \Delta\rho_{xy} \end{bmatrix} = \rho \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{13} & \pi_{14} & \pi_{15} & \pi_{16} \\ \pi_{21} & \pi_{22} & \pi_{23} & \pi_{24} & \pi_{25} & \pi_{26} \\ \pi_{31} & \pi_{32} & \pi_{33} & \pi_{34} & \pi_{35} & \pi_{36} \\ \pi_{41} & \pi_{42} & \pi_{43} & \pi_{44} & \pi_{45} & \pi_{46} \\ \pi_{51} & \pi_{52} & \pi_{53} & \pi_{54} & \pi_{55} & \pi_{56} \\ \pi_{61} & \pi_{62} & \pi_{63} & \pi_{64} & \pi_{65} & \pi_{66} \end{bmatrix} \cdot \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} \tag{3.5}$$

This result is then used to form the full resistivity matrix as shown in the expanded version of Equation 3.2:

$$\begin{bmatrix} E_x \\ E_y \\ E_z \end{bmatrix} = \rho \cdot \begin{bmatrix} J_x \\ J_y \\ J_z \end{bmatrix} + \begin{bmatrix} \Delta\rho_{xx} & \Delta\rho_{xy} & \Delta\rho_{xz} \\ \Delta\rho_{xy} & \Delta\rho_{yy} & \Delta\rho_{yz} \\ \Delta\rho_{xz} & \Delta\rho_{yz} & \Delta\rho_{zz} \end{bmatrix} \cdot \begin{bmatrix} J_x \\ J_y \\ J_z \end{bmatrix} \tag{3.6}$$

Due to the cubic symmetry of silicon, the piezoresistivity matrix π can be reduced to only three independent constants. The matrix becomes:

$$\begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{3.7}$$

with $\pi_{11} = 6.6 \times 10^{-11}$ m^2/N, $\pi_{12} = -1.1 \times 10^{-11}$ m^2/N and $\pi_{44} = 138.1 \times 10^{-11}$ m^2/N for p-Si.

In COMSOL, these equations are solved self-consistently: the mechanical stress is first computed using the structural mechanics module, and the resulting stress distribution is then used to compute changes in resistivity via the piezoresistivity tensor. This updated resistivity tensor feeds into the electrical simulation to calculate current flow and voltage distribution under applied loads.

3.2 Simulation setup

3.2.1 Simulation environment and physics interfaces

To simulate the piezoresistive cantilever, a finite element model was constructed using *COMSOL Multiphysics* with the *MEMS Module*, which offers built-in capabilities for modeling piezoresistive effects. A *3D* geometry was selected to fully capture the mechanical deformation and electrical response of the cantilever in space.

The piezoresistive effect can be modeled in *COMSOL* through one of three available physics interfaces:

- *Domain Currents*: Best suited for cases where the piezoresistive layer has significant thickness and its volumetric effects must be captured.
- *Boundary Currents*: Appropriate when the piezoresistive layer is very thin compared to the structural layer.
- *Shell Interface*: Used for thin shell structures where the piezoresistive layer is even thinner.

Given the thickness of the silicon layer in our design, the *Domain Currents* interface was selected to ensure that the volumetric contribution of the piezoresistor to resistance changes is properly modeled.

As the study focuses on equilibrium conditions and resistance changes under steady loading, a *Stationary Study* was chosen.

3.2.2 Geometry Construction

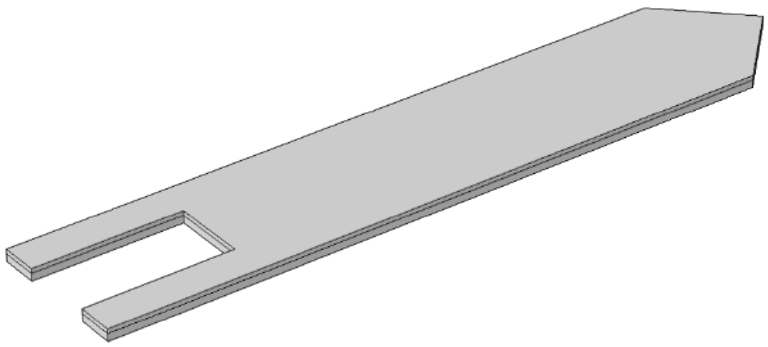


Figure 3.1: Geometry of the modeled cantilever for FEM simulation

The cantilever geometry is relatively simple, requiring only a few parameters to define its configuration:

1. **Base Geometry**: A rectangle is drawn in the x–y plane, with its base-end aligned at the origin and the longitudinal axis of symmetry along the x-axis.
2. **Chamfering**: Two corners at the free end of the rectangle are chamfered to represent the shape of the cantilever tip.
3. **Leg Cut-Out**: A second rectangle is created and subtracted from the base geometry to define the cantilever legs. The length and width of this rectangle determine the leg dimensions.

4. **Extrusion**: The resulting 2D shape is extruded along the z-axis to define the thickness of the silicon layer. This domain is assigned p-type silicon (p-Si) as the material.
5. **Silicon Nitride Layer**: A similar 2D sketch is created on a plane offset in the z-direction, corresponding to the thickness of the silicon layer. This layer is then extruded to represent the silicon nitride passivation layer and assigned the appropriate material properties.

The modeled cantilever geometry can be seen in Figure 3.1.

3.2.3 Boundary Conditions and Physics Configuration

After building the geometry, mechanical and electrical boundary conditions were defined:

- **Structural Mechanics**:
  - A *Point Load* is applied at the free end of the cantilever to simulate an external load.
  - A *Fixed Constraint* is applied to all faces at the base-end, anchoring the cantilever.
- **Electric Currents**:
  - The *Piezoresistive Material* is applied only to the silicon domain, representing the electrically active part of the cantilever.
  - The carrier number density is set to 5×10^{15} cm^{-3} to emulate the resistivity value provided by the wafer manufacturer.
  - A *Terminal* voltage of 1 V is applied to one cantilever leg, while the other leg is assigned to *Ground*.

3.2.4 Meshing and Solver Settings

An automatic physics-controlled meshing was used to ensure compatibility with the defined physics interfaces. The *finer* mesh size was selected to provide sufficient resolution at the legs without significantly increasing computational cost. Other configurations were left by default.

3.3 Simulation results and discussions

To investigate the influence of different geometrical parameters on the sensitivity of the piezoresistive cantilevers, a series of parametric sweep studies were carried out. In each simulation, one geometrical parameter was varied while the others were kept constant to isolate its effect on device sensitivity. The full set of parameters and the respective values used in this study are summarized in Table 3.1.

The electrical resistance of the cantilever was calculated by dividing the applied voltage by the resulting current computed at the electrical terminal of the device. To evaluate sensitivity to external force, the resistance was computed for two scenarios: in the absence of applied force, and under an applied point force of 1×10^{-7} N. The fractional change in resistance between these two conditions served as a metric for sensitivity.

Parameter	Start	End	Step
l_{leg} [µm]	5	100	5
w_{leg} [µm]	5	45	5
t_{Si} [µm]	1	5	0.5
$t_{Si_3N_4}$ [µm]	0.1	0.5	0.1

Table 3.1: Sweeping parameters for study of cantilever geometry.

Effect of Leg Length

The first parameter studied was the leg length, l_{leg}, while keeping the leg width w_{leg} = 15 μm, silicon thickness t_{Si} = 5 µm, and silicon nitride thickness $t_{Si_3N_4}$ = 0.4 µm constant. The results are shown in Figure 3.2.

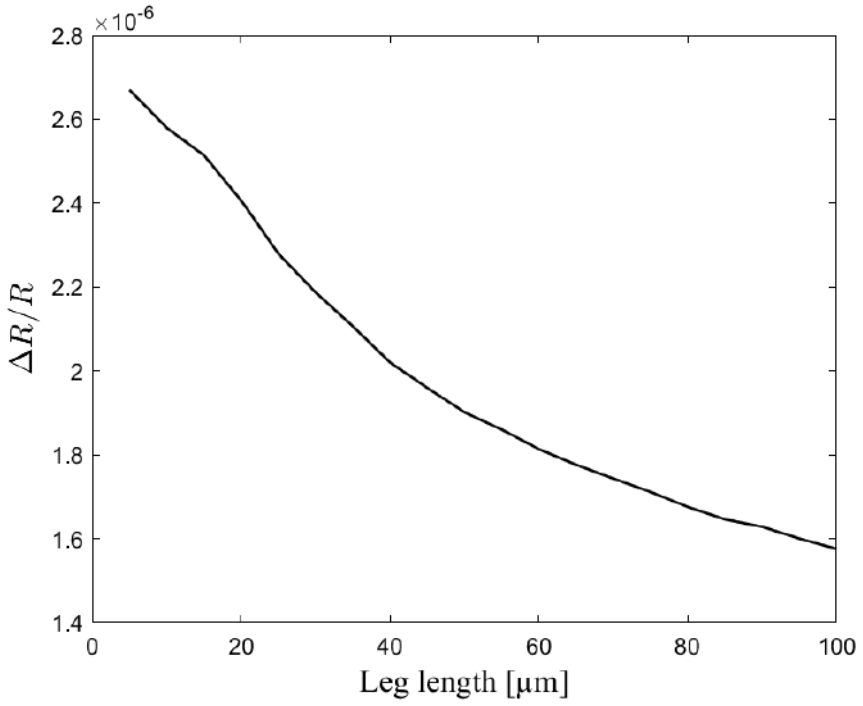


Figure 3.2: Fractional change in resistance as a function of leg length

It was observed that the fractional change in resistance decreases with increasing leg length. This behavior is consistent with theoretical expectations, as the piezoresistor length is related closely to the leg length. A longer piezoresistor reduces the relative change in resistance under mechanical loading, resulting in a smaller output signal. Thus, increasing leg length leads to reduced sensitivity.

Effect of Leg Width

Next, the leg width w_{leg} was varied while maintaining fixed values of l_{leg} = 100 µm, t_{Si} = 5 µm, and $t_{Si_3N_4}$ = 0.4 µm. The resulting change in resistance is plotted in Figure 3.3.

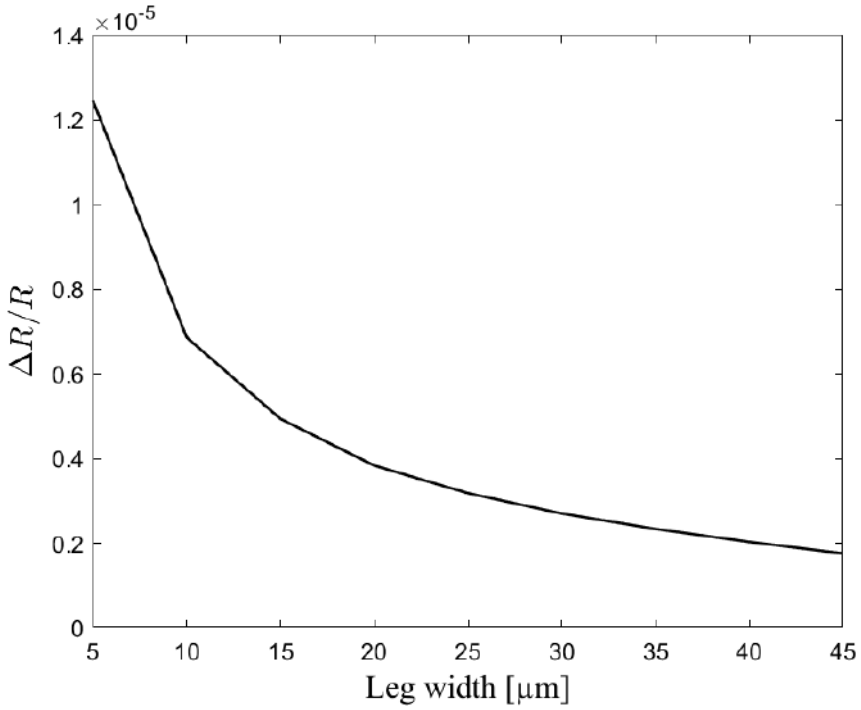


Figure 3.3: Fractional change in resistance as a function of leg width

The simulation results indicate that the fractional change in resistance increases rapidly as the leg width decreases. This can be attributed to the concentration of mechanical stress in narrower regions. Additionally, narrower legs are mechanically less stiff, meaning that under the same applied force, they experience greater deformation and thus more stress. Both effects combine to increase the output signal significantly for narrower legs.

Effect of Silicon Thickness

The third parameter varied was the thickness of the silicon layer t_{Si}, while keeping l_{leg} = 100 µm, w_{leg} = 15 µm, and $t_{Si_3N_4}$ = 0.4 µm constant. Figure 3.4 shows the resulting data.

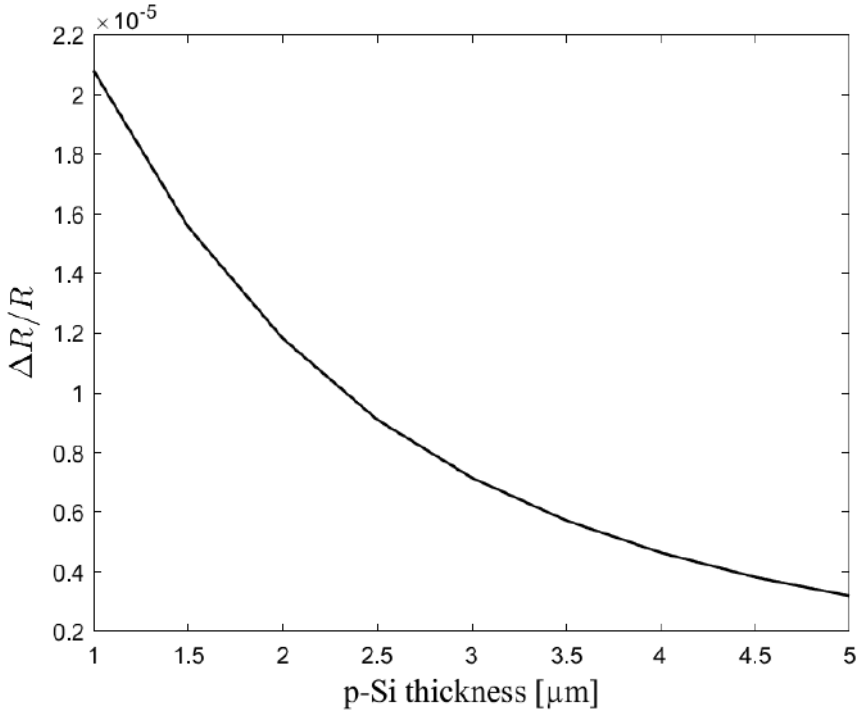


Figure 3.4: Fractional change in resistance as a function of silicon layer thickness

As expected, the sensitivity increases as the silicon layer becomes thinner. This relationship is approximately exponential. The thickness of the silicon layer defines the thickness of the piezoresistor itself. For a constant silicon nitride thickness, reducing the silicon thickness moves the mechanical neutral axis away from the center of the piezoresistive region. This shift increases the piezoresistive efficient factor β^*, resulting in greater sensitivity.

Effect of Silicon Nitride Thickness

Finally, the thickness of the silicon nitride layer $t_{Si_3N_4}$ was varied while the other parameters were fixed at l_{leg} = 100 µm, w_{leg} = 15 µm, and t_{Si} = 5 µm. The resulting data is presented in Figure 3.5.

The results show a nearly linear increase in sensitivity with increasing nitride thickness. The explanation for this is similar to that of the silicon thickness: a thicker nitride layer alters the position of the neutral axis relative to piezoresistor center line and thereby increases the sensor's sensitivity.

In summary, from the parametric studies conducted, it is evident that the leg width and the silicon thickness are the most influential factors affecting cantilever sensitivity.

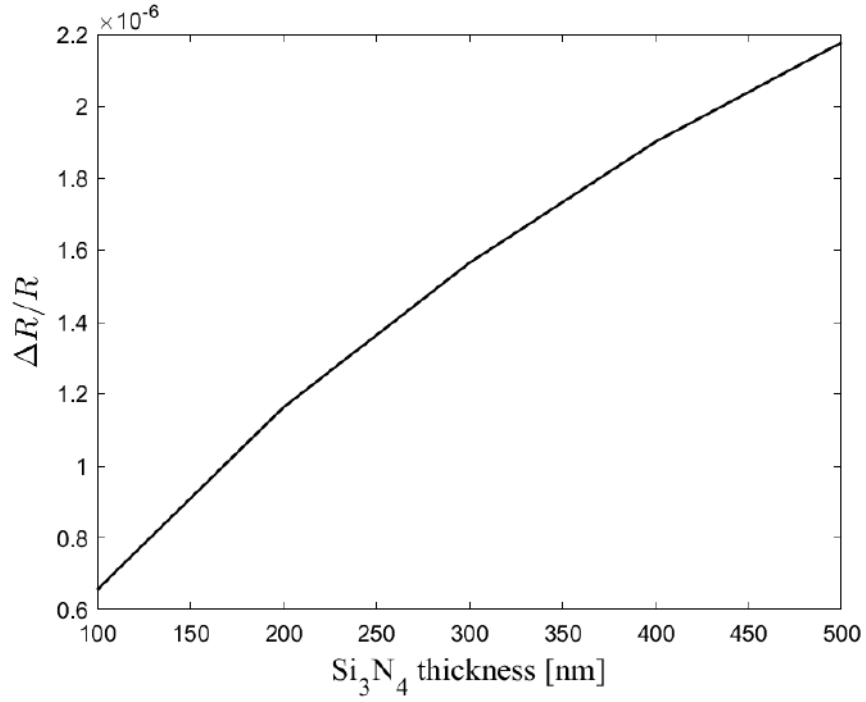


Figure 3.5: Fractional change in resistance as a function of silicon nitride layer thickness

Narrower and thinner piezoresistors consistently yield higher resistance changes under applied force increasing the sensitivity accordingly.

While it is always advantageous to minimize piezoresistor width and thickness to maximize sensitivity, practical constraints must also be considered. Fabrication limitations such as etch uniformity, photolithographic resolution, and alignment precision impose constraints on these dimensions. Additionally, electrical consideration such as total resistance may necessitate a compromise between sensitivity and and signal-to-noise ratio. Therefore, optimal design requires careful balancing of mechanical, electrical, and manufacturing constraints.

4 Fabrication and characterization of piezoresistive cantilevers

The need to tailor cantilevers to meet specific measurement requirements has motivated the development of custom-designed silicon piezoresistive cantilevers. This chapter outlines the fabrication process of the designed cantilevers and presents the experimental characterization of the fabricated devices. Both the fabrication challenges and the performance evaluation, including electrical and mechanical tests, are discussed in detail to assess the viability of the design for targeted applications.

4.1 Cantilever design

The final design of the piezoresistive microcantilevers was developed based on the theoretical analysis presented in Chapter 2 and the simulation results discussed in Chapter 3. It incorporates several key features aimed at optimizing the sensing performance. A schematic representation of the device layout is shown in Figure 4.1.

A rectangular opening was introduced into a standard cantilever geometry, such that the whole cantilever is suspended from the substrate via two narrow supporting legs. This configuration serves a dual purpose. First, it enforces a U-shaped current path through the piezoresistive material, ensuring that the electrical current flows through the regions experiencing mechanical stress. This is essential for enabling the piezoresistive sensing functionality. Second, it enhances sensitivity by concentrating the stress in the narrow legs, where the piezoresistors are located.

To enable the measurements of resistance change and suppress common-mode noise sources, three reference resistors were integrated onto the same chip. These reference resistors were fabricated by etching the same geometry into the device layer as the active piezoresistive elements. This design ensures that the reference resistors are subject to identical environmental conditions, such as temperature fluctuations, thus allowing for effective cancellation of noise.

In addition to the electrical contacts required for sensing, two additional electrodes were incorporated onto the cantilever structure to support the requirements of the QTM experiment. These electrodes extend along the cantilever body all the way to the free end and are intended to serve as contacts for tunneling or electrostatic control in QTM operation.

The cantilever itself is composed of two functional layers: a doped silicon layer that serves as the piezoresistive transducer, and a silicon nitride layer positioned above it. The inclusion of the silicon nitride layer plays a critical role. It shifts the neutral axis of bending away from the centerline of the piezoresistive layer, thereby increasing the mechanical strain experienced by the piezoresistor and enhancing the overall sensitivity. Additionally, the silicon nitride layer acts as an electrical isolation barrier, separating the QTM electrodes from the piezoresistive sensing circuit.

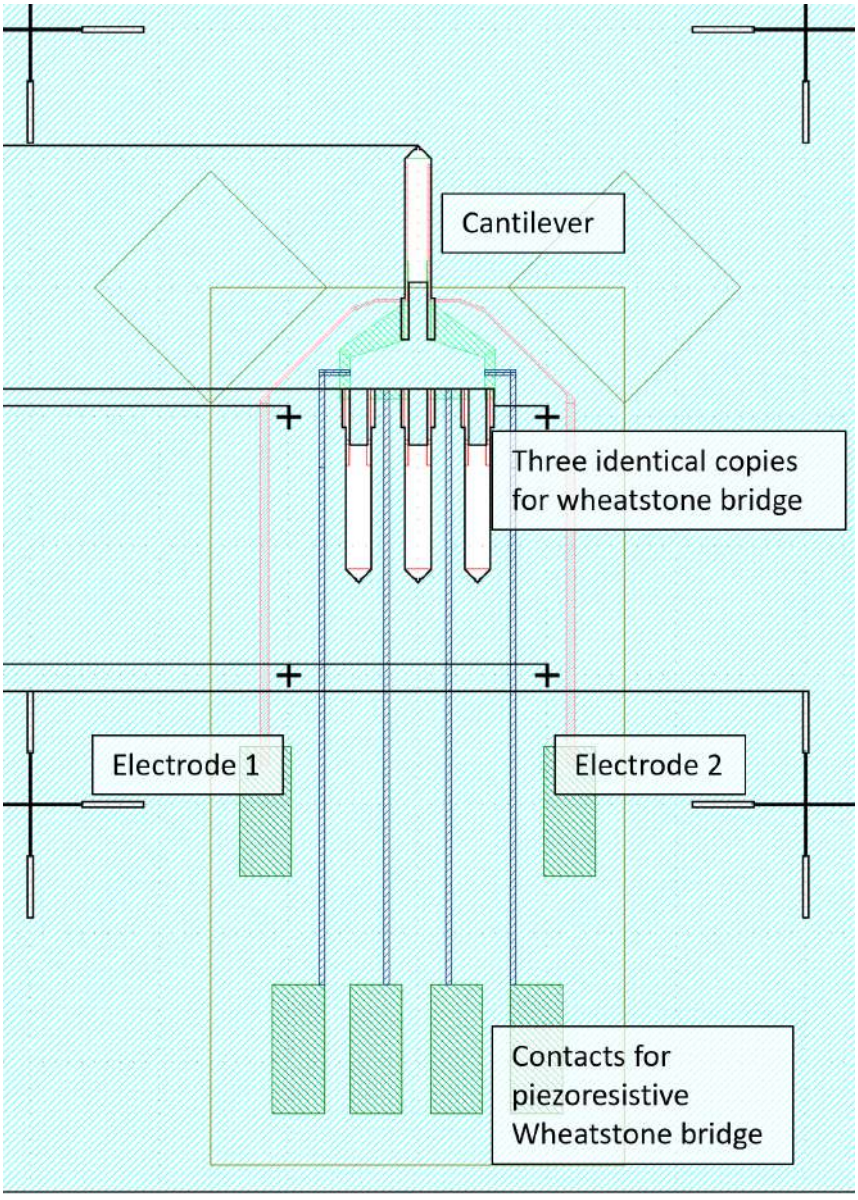


Figure 4.1: Schematic illustration of the cantilever design with integrated piezoresistive sensor, Wheatstone bridge for readout and additional electrodes for QTM experiments.

The overall chip dimensions were set to 1600 µm by 3300 µm. This size was chosen to ensure compatibility with standard AFM holders and the custom-designed PCB, while still providing sufficient space to integrate a full Wheatstone bridge and bonding pads on-chip. Additionally, the compact form allowed three cantilever devices to be fabricated on a single diced chip, maximizing efficiency in each fabrication run.

The cantilever's total length and width were fixed at 500 µm by 100 µm. The design of the legs is critical from both sensitivity and fabrication standpoint. A leg length of 100 µm was selected to achieve a balance between sensitivity and fabrication reliability. Shorter legs provide slightly higher sensitivity, but if they are too short, there is a high risk that the backside-etched trench will miss the legs entirely, disabling the sensing functionality completely. Similarly, the leg width was set to 15 µm—a value that ensures a reasonable trade-off between sensitivity and electrical performance. Narrower legs would enhance stress concentration and thus sensitivity, but at the cost of higher resistance, which can lead to increased electrical noise. Additionally, a width of 15 µm provides sufficient space to accommodate at least one metal electrode, which is essential for the intended use in QTM.

The thicknesses of the doped silicon and silicon nitride layers are defined by the specifications of the SOI wafer used in fabrication and were kept fixed throughout the design process at 5 µm and 0.4 µm, respectively. Although it would have been theoretically possible to further increase the sensitivity by thinning the silicon layer from the wafer backside, this approach was avoided. An additional backside etching would introduce significant complexity to the fabrication sequence, making it less robust and more difficult to reproduce consistently within the existing process capabilities.

It is important to emphasize that this design represents the first prototype iteration of the cantilever for QTM experiments. Further optimization may be required based on the performance of fabricated devices. Adjustments in device geometry or materials could be made in future iterations to improve performance, particularly in cryogenic measurement environments.

4.2 Fabrication techniques

Since the fabrication techniques utilized for piezoresistive cantilever are commonly used and well known, they will be only briefly reviewed here in this section.

4.2.1 Photolithography

Photolithography refers to the process that makes use of light to define patterns on a light sensitive material called photoresist. Photolithography process starts with a temporary coating of a substrate with a layer of resist (positive or negative) followed by baking. The substrate is then exposed to UV light through a mask changing the chemistry of the exposed areas. Next, a developer commonly a base solution is used to remove the exposed areas for positive photoresists or unexposed areas for negative photoresists. The pattern on the resist can be subsequently transferred into the substrate using further

microstructuring techniques, e.g. etching or lift-off. Schematic of photolithography process is illustrated in Figure 4.2.

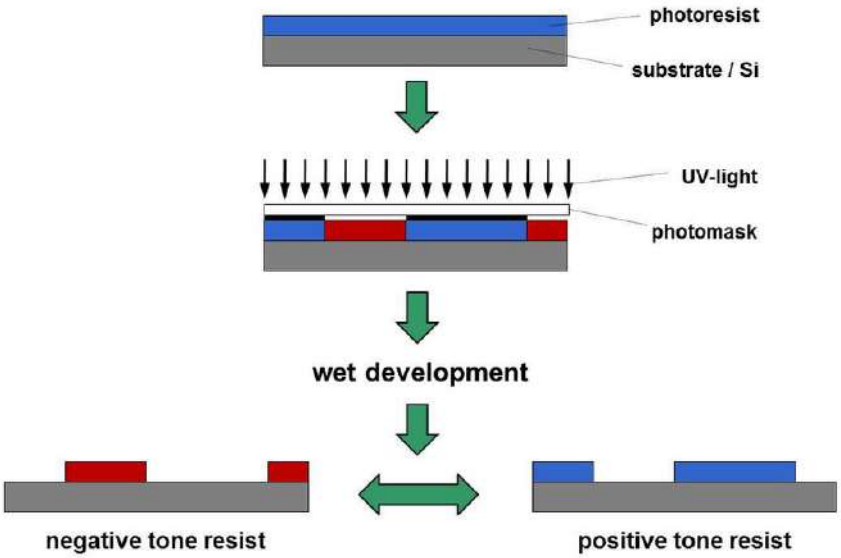


Figure 4.2: Schematic illustration of process flow for photolithography: applying of photoresist, UV exposure and development. Adapted from [28].

A photoresist typically consists of three main ingredients: a base resin, a photoactive substance and a solvent. Photoresists may also include other components such as adhesion promoters and anti-oxidizing agents. The positive resist S1813 from Microposit will be taken as an example to understand the chemical processes behind photolithography. The resin of S1813 is Novolak, a polymerized phenol made of formaldehyde and phenol. Its photoactive compound belongs to the Diazonaphtoquinone (DNQ) group. Their presence in photoresist reduce the solubility in alkaline solution to one or two orders of magnitude below that of pure phenolic resin. During exposure to appropriate wavelengths, DNQ absorbs UV light forming a ketene intermediate. The ketene reacts with water to form carboxylic acid derivative (Fig. 4.3. This acid his acid is highly soluble in alkaline developer, enabling pattern development of the resist.

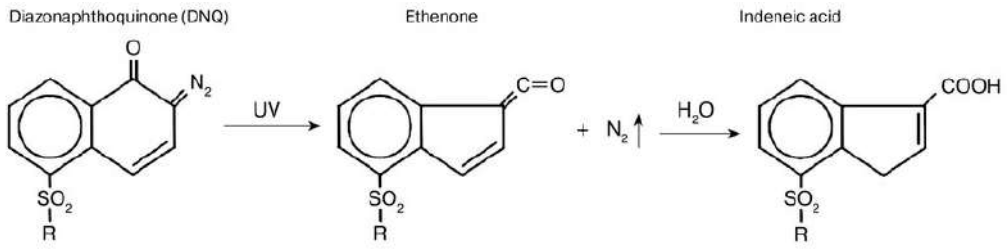


Figure 4.3: Chemical decomposition of DNQ under exposure of UV light. Adapted from [29].

The limit of the size of the patterns that can be made with photolithography is called the diffraction limit ($\approx \lambda/2NA$) where NA is the numerical aperture of the lens used to condense the light and λ is the wavelength of the light used.

4.2.2 Lift-off process

The lift-off technique is a widely used method to create patterned thin films, particularly metal layers, on substrates. To do lift-off, we first apply the photoresist and do conventional photolithography. The patterned resist will act now as a sacrificial layer. A thin film (usually a metal) is deposited over the entire surface — both on the resist and in the exposed substrate areas. The substrate is then immersed in a solvent (e.g., acetone) that dissolves the resist. The material deposited on top of the resist is "lifted off", while that in the patterned regions remains. This is shown schematically in Figure 4.4.

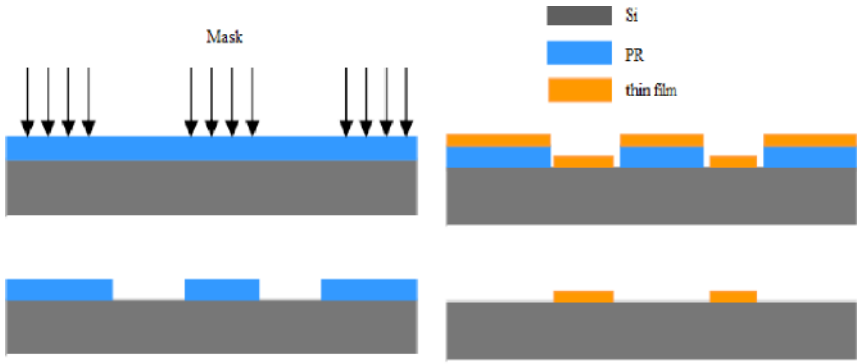


Figure 4.4: Schematic illustration of lift-off process for thin film patterning. Adapted from [30].

The lift-off method is ideal for materials that are difficult to etch, allows for high-resolution patterning with undercut resists, and avoids damage to sensitive layers since no aggressive post-processing is needed. However, it is generally limited to thin films, not compatible with conformal deposition methods, and may leave residues if not properly optimized.

4.2.3 E-beam evaporation

For lift-off, we would need to deposit the desired material onto the substrate.

E-beam evaporation is a physical vapor deposition technique widely used to deposit high-purity thin films in microfabrication. It involves bombarding a solid source material, called a "target", with a focused, high-energy electron beam under high vacuum. The energy from the beam heats the material to its evaporation point, causing atoms or molecules to leave the target and condense onto a substrate, forming a thin film. Figure 4.5 depicts the schematic of a e-beam evaporation system.

The process begins with placing the source material in a crucible, typically made from tungsten. An electron gun, positioned at a distance, generates a beam that is electromagnetically directed onto the target. The interaction between the high-energy

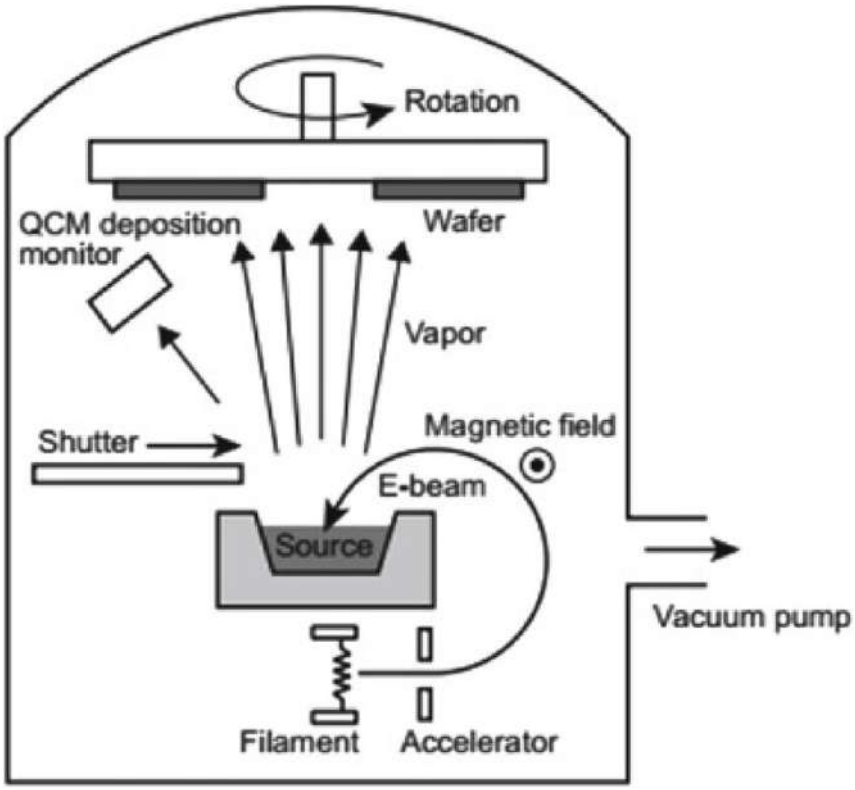


Figure 4.5: Illustration of e-beam evaporation system. Adapted from [31].

electrons and the material surface causes localized heating and vaporization. Because the beam can be tightly focused, very high temperatures can be achieved, allowing for the evaporation of materials with high melting poinit, e.g. tungsten or titanium.

E-beam evaporation occurs under high vacuum to ensure a long mean free path for the evaporated atoms and to prevent contamination. The evaporated atoms travel linearly and deposit on substrates placed above the target. Therefore, e-beam evaporation is considered to be more suitable technique for lift-off due to its unidirectional film growth characteristics.

4.2.4 Reactive ion etching

Reactive Ion Etching (RIE) is a dry etching technique used in micro- and nanofabrication to selectively remove materials from a substrate using a combination of chemical reactions and physical ion bombardment in a plasma environment. It provides anisotropic etching, making it essential for defining fine patterns in microelectronics and MEMS.

RIE takes place in a low-pressure chamber where a gas (or mixture of gases) is introduced and ionized using a radio-frequency (RF) electric field, typically at 13.56 MHz. The resulting plasma contains reactive species, e.g. radicals and ions. Due to electrons having higher mobility than the ions, after ignition, the substrate acquires a negative charge, and thus the sample set on the electrode is imposed to ion bombardment of the

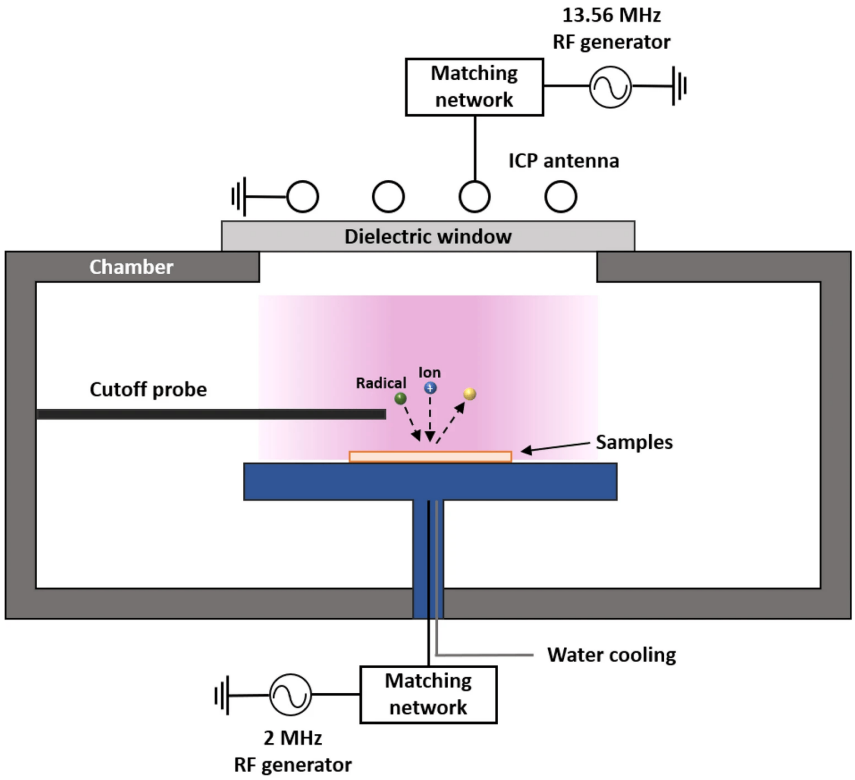


Figure 4.6: Schematic illustration of reactive ion etching process. Adapted from [32].

positive ions. Charging of the substrate is also called the self-bias voltage. These ions accelerate vertically toward the surface, enabling directional etching. Simultaneously, reactive radicals chemically interact with the material, enhancing the removal process. This combination of physical sputtering and chemical reactions enables highly controlled and anisotropic etching. Generally, there are six basic main process parameters that can be used to modify the plasma properties, and thus, affect the etching results: gas chemistry, RIE power, ICP/CCP power, process pressure, process temperature, and the flow rate of gases.

Typical gas for the etching of SiO_2 are fluorinated hydrocarbons ($C_xH_yF_z$), whereas typical gas for the etching of Si are clorinated and fluorinated compounds. The etching mechanisms are presented exemplary below for CHF_3 and SF_6. First, active species are generated in plasma discharge by electron-impact:

$$\begin{aligned} CHF_3 + e^- &\longrightarrow CF_3{}^* + H^* + e^- \\ CHF_3 + e^- &\longrightarrow CF_2{}^* + HF + e^- \\ CHF_3 + e^- &\longrightarrow CF^* + HF + F^* + e^- \end{aligned}$$

$$e^- + SF_6 \longrightarrow e^- + SF_5{}^* + F^*$$

Then the removing of material occurs through formation of volatile Si compounds:

$$SiO_2 + 4F^* \longrightarrow SiF_4 + O_2$$

$$Si + 4F^* \longrightarrow SiF_4$$

CF_x radicals tend to form fluorocarbon polymers and passivate the surfaces, leading to a etching selectivity of SiO_2 over Si. It also has to be noted that, the more oxygen is present in plasma, the higher the removal rate of the resist. Gases like oxygen can be added as a scavenger, i.e. it can react with fragments of CF_x and SF_x, and simultaneously keeping fluorine concentration high in the plasma, thus increasing the etching rate. Nevertheless, oxygen also reacts with resists, which can decrease selectivity between the etched material and resist.

4.2.5 Anisotropic wet etching

Anisotropic wet etching refers to the chemical removal of silicon in a directionally dependent manner, where the etch rate varies with crystal orientation. This process is widely used in MEMS fabrication and microstructuring of silicon due to its ability to produce well-defined, angled features such as V-grooves and pyramidal pits.

The most commonly used etchants for anisotropic etching are aqueous alkaline solutions such as potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). These solutions preferentially etch certain silicon crystal planes much faster than others. For example, in a (100)-oriented silicon wafer, the <100> planes etch rapidly, while the <111> planes are much more resistant, resulting in angled sidewalls at 54.7°.

The etching mechanism involves hydroxide ions attacking silicon atoms, breaking Si–Si bonds at the surface. The etch proceeds more rapidly on atomically rougher planes like <100>, because they have higher atomic density of dangling bonds, whereas <111> planes have closely packed atoms and fewer dangling bonds, making them chemically less reactive. The reaction in KOH etching can be summerized as:

$$Si + 2OH^- + 2H_2O \longrightarrow SiO_2(OH)_2{}^{2-} + 2H_2$$

The etch behavior of KOH is strongly influenced by several process parameters, which must be carefully controlled to achieve desired results. Temperature is one of the most critical parameters with increasing etch rate with temperature. At around 70-80°C, KOH provides a good balance between etch rate and surface smoothness. Higher temperatures accelerate etching but may also increase roughness and reduce mask selectivity. The concentration of KOH in the aqueous solution affects both etch rate and anisotropy. Higher concentrations decreases the etch rate up as water is needed for the chemical reaction. An optimal concentration around 30% is often used to balance rate and directional control. Agitation or stirring enhances uniformity and etch rate by improving the removal of reaction byproducts, e.g. hydrogen bubbles, from the wafer surface. Proper agitation

prevents local etch rate variations and ensures cleaner profiles. KOH etching also exhibits a very high etching selectivity, that's why SiO_2 and Si_3N_4 is usually used as etching masks.

4.3 Experimental challenges

Before and during the fabrication of the cantilever, we encountered several experimental challenges that required resolution. This section presents those challenges along with the strategies we employed to overcome them.

4.3.1 Front-to-back alignment

The cantilever beam fabrication process relies on a double-sided micromachining approach, which requires precise alignment between the patterns on both sides of the wafer. Front-to-back alignment is typically achieved using commercial mask aligners equipped with infrared illumination or dual-sided optical systems. However, such equipment is costly and not available in our cleanroom. Consequently, we tried alternative methods to align the structures on one side of the wafer to those on the opposite side.

To evaluate the tested method, we designed a test structure to measure the alignment accuracy. On the front side of the wafer, a cross was etched into the handle layer. On the backside, a square window was opened via KOH etching, large enough to expose the buried oxide (BOX) layer. The relative position of the square window and the cross can be observed from the front side using a microscope. In the case of perfect alignment, the cross should be precisely centered within the square. Any deviation between these two features serves as a measure of the alignment accuracy of our methods.

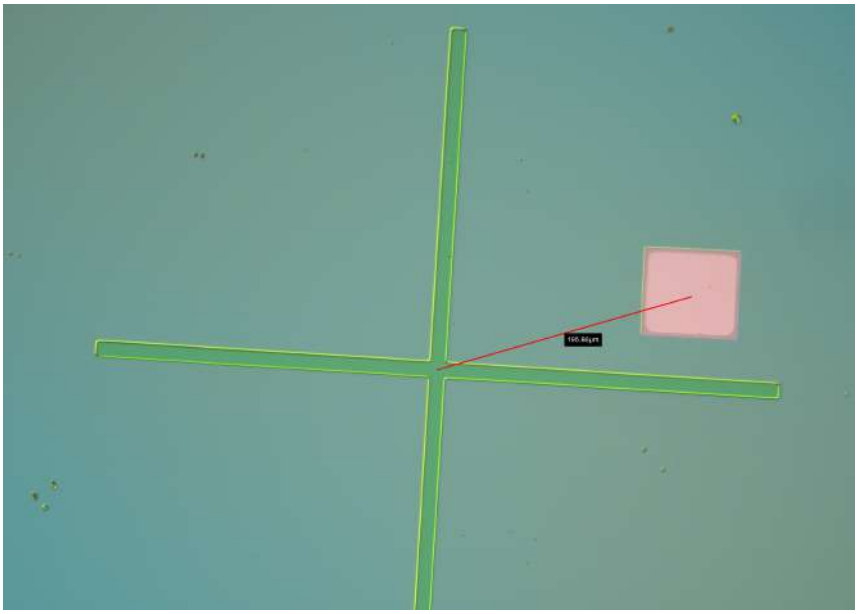
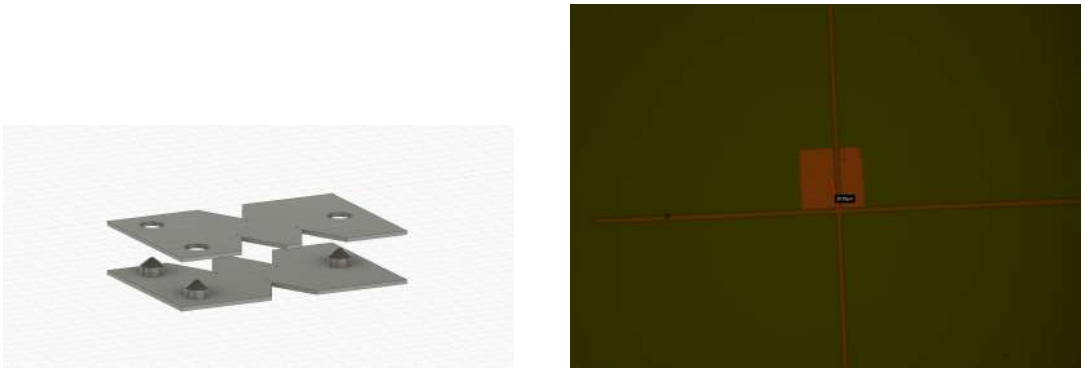


Figure 4.7: Measured deviation using the corners as alignment marks.

The first method we attempted involved using the corners of the chip as alignment marks. However, this approach proved to be inaccurate, as the deviation between the front- and backside features exceeded 100 µm, as shown in Figure 4.7. The inaccuracy was primarily due to imperfect chip dicing even with a chip dicer. Under the microscope, the chip edges appeared rounded or fractured, making them unsuitable as reliable alignment references.

In the second method, we fabricated a 3D-printed shadow mask to define alignment marks on both sides of the chip. The 3D design of the mask is shown in Figure 4.8a. The mask consists of two parts with aligned circular openings, which, when assembled, create through-holes at matching positions on both sides. The chip is sandwiched between these two parts, and a thin metal film is deposited. The metal reaches the wafer surface only through the open windows, forming alignment dots on both sides. These metal dots serve as reference marks for the subsequent double-sided micromachining process.



(a) (b)

Figure 4.8: (**a**) 3D design of the shadow mask for front-to-back alignment. (**b**) Measured deviation using the 3D-printed shadow mask for alignment.

The second method achieved an alignment accuracy between 20 and 40 µm (Fig. 4.8b), which is a significant improvement over the first approach. Although we attempted to optimize the mask design to reach an accuracy better than 10 µm, these efforts were unsuccessful. The limited accuracy of this method is likely due to the resolution of the 3D printing process and the deformation or bending of the printed parts. Nevertheless, we successfully fabricated a suspended cantilever beam using this alignment technique, and the result was sufficiently precise for our application. Therefore, we decided to adopt this method for the final fabrication.

4.3.2 Underetch of convex corner in KOH

Undercutting of convex corners in KOH anisotropic etching is a well-known phenomenon, especially when working with crystalline silicon wafers. When a mask features convex corners, the <111> planes at those locations are gradually etched away. If the etching continues to completion, the underlying material is fully removed, causing the masking layer to become suspended over a V-shaped groove (Fig. 4.9). A likely explanation for

this behavior is that <111> planes typically possess a single dangling surface atom bond, making them relatively slow to etch. However, at convex corners where two <111> planes intersect, two dangling bonds are present, increasing the chemical reactivity at these sites. As a result, these regions are etched more rapidly, exposing other crystallographic planes with higher etch rates and leading to undercutting. This characteristic poses a challenge in cantilever fabrication, as a well-defined straight edge is required to precisely control the cantilever length and ensure proper suspension.

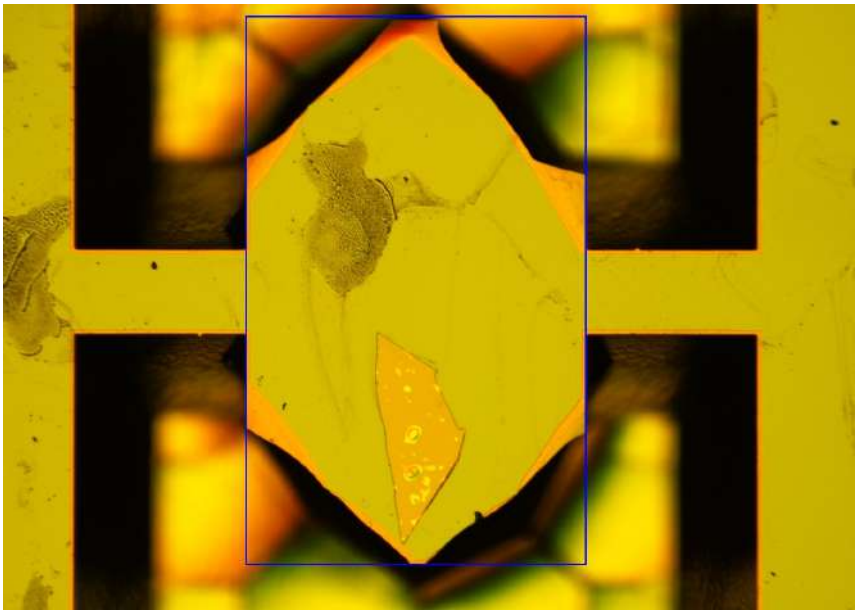


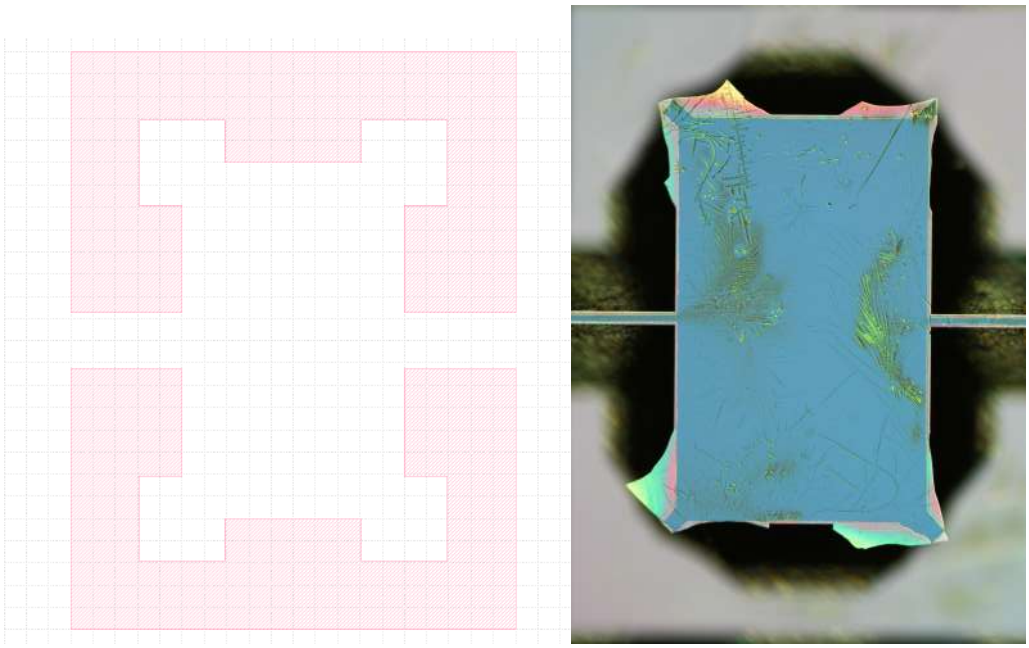
Figure 4.9: Microscope image of etched test sample showing undercutting of convex corner, blue rectangle indicates masked area.

Several strategies can be employed to minimize or prevent undercutting at convex corners during KOH anisotropic etching of silicon. These include the addition of chemical additives such as isopropanol or surfactants, or the use of alternative etchants. However, one of the simplest and most widely used approaches is the incorporation of so-called compensation structures into the mask layout (Fig. 4.10a). To determine the appropriate dimensions of these structures, we conducted a series of tests. Our experiments showed that a square compensation structure with a minimum size of 750 µm is necessary to effectively minimize the impact of undercutting as can be seen in Figure 4.10b.

4.3.3 Frontside protection during KOH etch

During wet etching processes, protecting the front side of a substrate is critical to prevent unintentional material removal and to maintain the integrity of the cantilever.

Front side protection can be achieved through several methods. A common approach is the application of a chemically resistant protective layer. The most effective protective layer materials for KOH etching are Si_3N_4 or SiO_2, due to their excellent resistance to alkaline solutions. However, depositing these films requires chemical vapor deposition,



(a) (b)

Figure 4.10: (**a**) Compensation structure design used to minimize the undercutting effect. (**b**) Microscope image of etched sample with compensation structures showing improved result.

which is not available in our cleanroom facility. Additionally, the removal of Si_3N_4/SiO_2 layers after etching can be problematic and potentially damaging to the substrate.

As an alternative, we tested the commercial polymer-based protective resist PC5040 from Allresist, which can be easily applied by spin coating and subsequently removed through oxygen plasma ashing. However, the results were not promising, as the resist began to detach after only a few hours of exposure to the KOH solution.

We then developed a customized sample holder for the KOH etching process, designed to protect the front side of the sample. The holder is made out of teflon and using two O-ring pressed against the sample to prevent contact with the etchant (Fig. 4.11). This approach yielded partial success, though in some cases the seal was imperfect, leading to occasional leakage.

Ultimately, we adopted a hybrid method combining the polymer-based protective coating with mechanical sealing using the custom sample holder. This approach offered improved front side protection and better process reliability.

Figure 4.11: 3D model of the sample holder using to protect patterned front side during wet etching.

4.4 Fabrication procedure

The cantilevers were fabricated on 4“ silicon-on-isolator (SOI) wafers. A 1 µm (±5%) thick layer of silicon oxide (BOX layer) is sandwiched in between two layers of single crystalline silicon. The upper layer (device layer) is used to form the cantilevers and is 5 µm thick. The bottom layer (handle layer) gives the wafer its structural stability and has a thickness of 380 ± 20 µm. The device layer has (100) crystal orientation and is doped with boron atoms, with a resistivity of 1-30 Ωcm. Both side of the wafer are polished and covered with an additional 400 nm thick silicon nitride layer. SOI wafers were chosen instead of bulk silicon wafers as the BOX provides an effective stopping layer for the etches that define the cantilevers. The sensitivity of the cantilever is also determined by the thickness and dopant concentration of device layer. Thus it is crucial to choose the right SOI-wafer for fabricating of desired piezolevers. The general process flow can be seen in Figure 4.12.

4.4.1 Dicing and depositing alignment marks

The first step of the fabrication is to dice the wafer into 15 cm by 15 cm chips by a wafer-dicer. This step was performed to ensure the chip fits inside the holder for KOH etching discussed in section 4.3. It is necessary to thoroughly clean the wafer chips before the next fabrication steps to remove or reduce any potentially preexisting contamination of the substrate, especially after breaking the wafer because of small wafer particles that are created with every break during the cleaving process. Contaminated samples are more likely to have defects or inhomogeneities in the photoresist layer after spin coating. This was done by sonication of the chips in an acetone bath for 5 minutes, followed by isopropanol to remove contaminated acetone before it can form streaks on the substrate. The cleaning was finalized by doing oxygen ashing for 2 minutes. We always performed cleaning prior to spinning resist, but for brevity, mention it once here.

The alignment marks are deposited using the 3D-printed shadow mask as discussed in previous section. The chip was secured onto one half of the mask by double-side carbon tape. The two parts were then brought into place and fixed together using kapton tape.

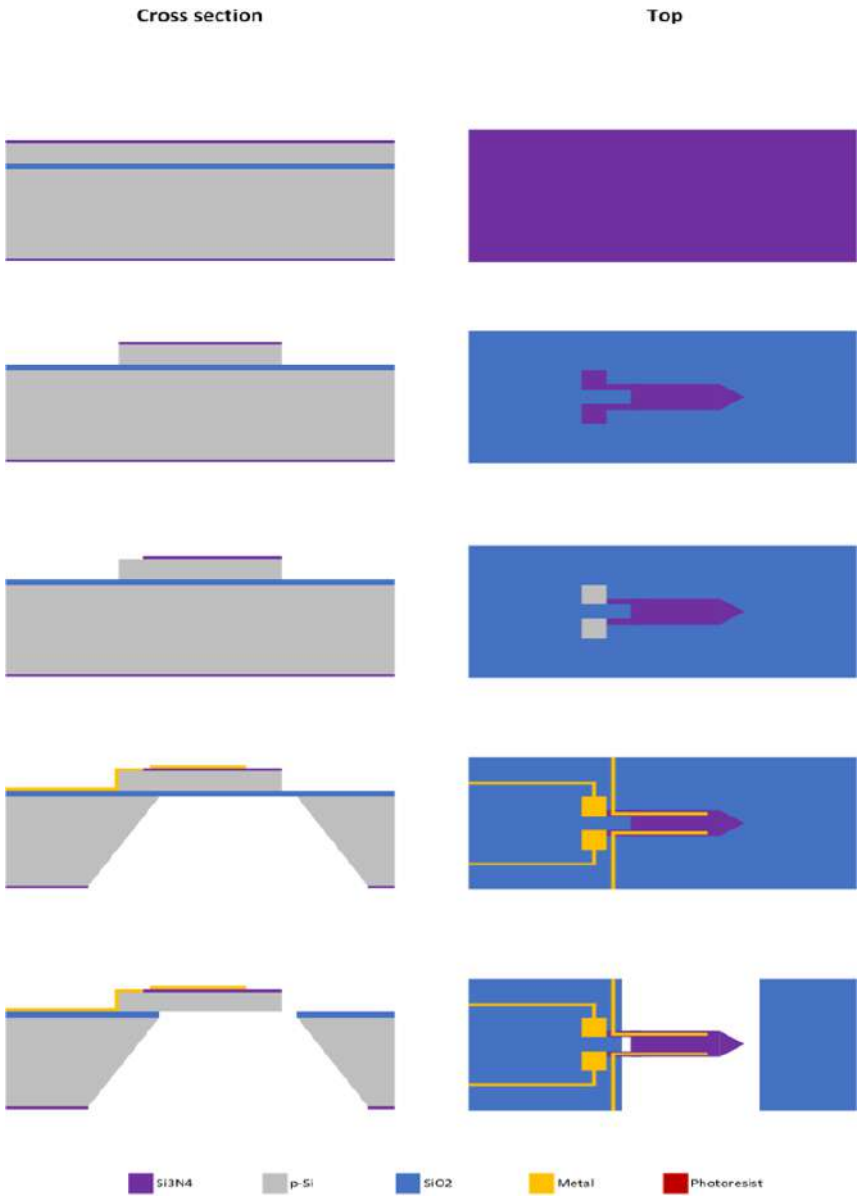


Figure 4.12: Overview of the process flow for fabrication of piezoresistive cantilever: Dicing of SOI wafer, definition of the cantilever shape into device layer, etching of the contact windows, deposition of electrical contacts, release of the cantilever.

It was then loaded into the ultra-high-vacuum evaporator. Approximately 50 nm thick layer of chromium was evaporated onto both sides of the sample to ensure visibility when doing aligning with the camera of the lithography system.

4.4.2 Patterning of front side

After initial preparation of the chips, we started with structuring the front side of the chip first. This process consists of three photolithography steps together with two dry etching steps to define the piezoresistive cantilever shape, three other resistors for the Wheatstone bridge and the metal traces as well as the electrodes. In this work, all photolithography were done using Microposit S1813 positive-tone photoresist.

The first photolithography was performed to define the shape of the cantilever and three identical resistors for the Wheatstone bridge. Four finer marks were also created for better alignment in subsequent processes. The photomask design of the first photolithography is shown in Figure 4.13. The photoresist was spun onto the sample at 4000 revolutions per minute for 45 seconds and an acceleration of 2000 $1/s^2$. The sample was then baked on a hot plate at 105°C for 2 minutes and left for cool-down and rehydration in air for few seconds. The exposure of the photoresist was done using Heidelberg µMLA maskless aligner. The structure was first positioned on the sample using front-to-back alignment marks created in previous step. An exposure dose of 400 mJ/cm^2 at +65 oAF was used. The resist was developed by submerging the sample in Microchemicals AZ 2026 MIF metal ion free developer for 40 seconds, and subsequently washed in deionized water to halt the development process. In the following, the recipe remains the same for other lithography steps, otherwise variations to the recipe will be provided.

Using the patterned resist as a soft mask the outline of the cantilever could be defined by dry etching into the device layer. We used a Sentech SI500 RIE-system for this purpose. This process again comprises of two substeps. First, the silicon nitride layer was etched in pure CHF_3 gas to increase selectivity to the resist mask, at 1 Pa pressure and a flow of 50 sccm for 9 minutes. Both RF and source power were at 100 W. This was followed by a second etch in a gas mixture of SF_6 and O_2 at 5 Pa for 15 minutes. The ratio of two gases in the mixture was SF_6:O_2 = 4:1, which corresponds to flow rates of 40 and 10 sccm respectively. An excessive etch duration was chosen to ensure that the silicon was etched away completely and consequently to prevent any short between the Wheatstone elements. It has to be noted that the newly created marks should be used to align the structure at front side hereafter.

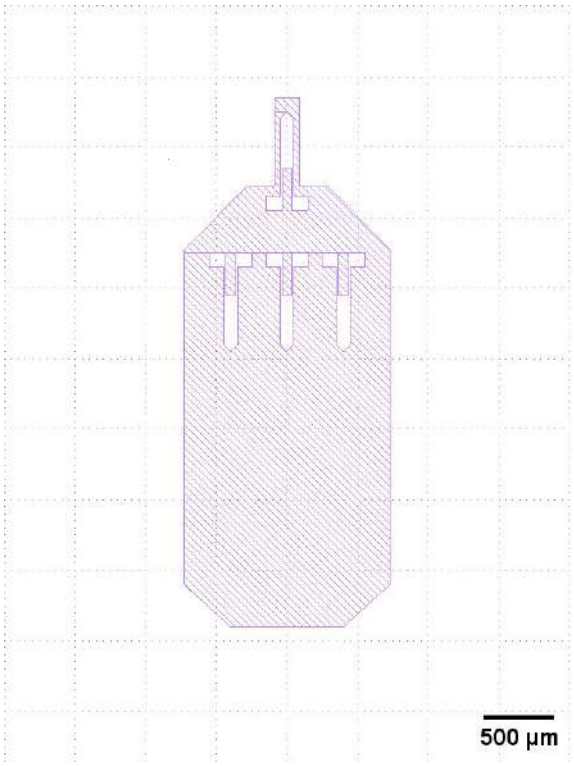
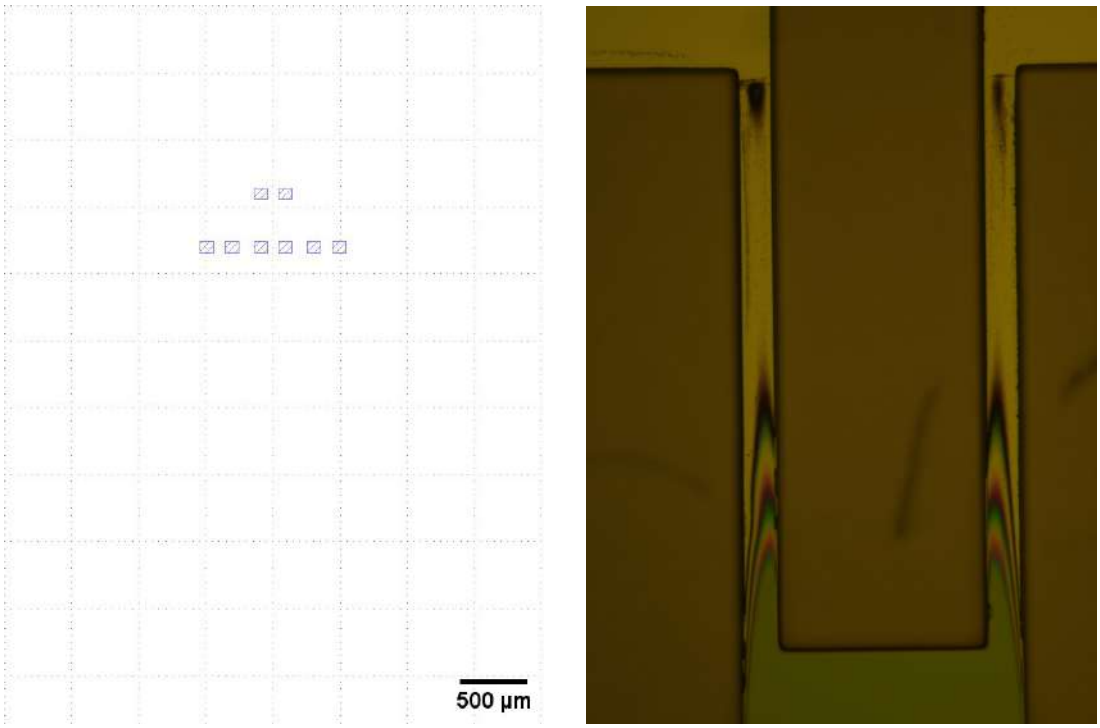


Figure 4.13: Photomask pattern of the first photolithography step.

After the beam structures had been formed, the wafer was cleaned in acetone/isopropanol. In the second lithography step (Fig. 4.14a) contact windows were patterned and opened by a subsequent dry etching of silicon nitride using the same recipe as before, to allow for connection of resistors with metal electrodes. The only change here was that the photoresist was spun at 3000 revolutions per minute to achieve a slightly thicker mask. The reason for this is when resist is spin coated on an already structured wafer, it can not be deposited homogeneously over the whole sample. It was observed that resist was thinner at the cantilever legs. This could lead to undesirable etch of silicon nitride at those areas and consequently to defective devices (Fig. 4.14b).



(a) (b)

Figure 4.14: (**a**) Photo mask of the second lithography step. (**b**) Undesired etching of silicon nitride at the cantilever legs after etching of contact windows.

Finally, the electrical connections were made by the third photolithography and a lift-off process (Fig. 4.15). This should be done immediately after opening the contact windows without any pretreatment to minimize native oxide growth, since a HF dip could have damaged the BOX layer. The pattern was transferred onto the resist with a standard lithography process. A chromium/gold thin film was then evaporated onto the sample for the electrodes. The thickness of the metal thin films were 5 nm and 60 nm respectively. For lift-off procedure, the sample was placed in a glass beaker containing acetone at 50°C. A syringe can be used to accelerate the removal of excess metal films. The sample was then cleaned in isopropanol and blow-dried with nitrogen gun.

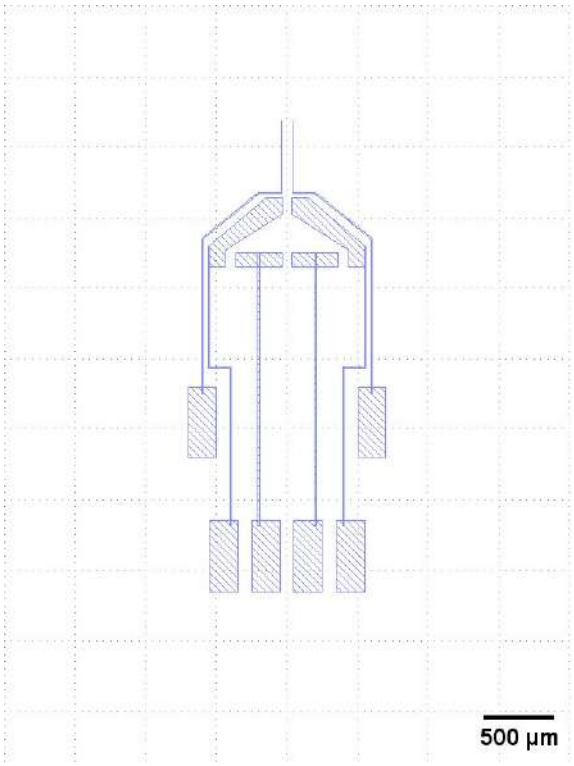


Figure 4.15: Photomask pattern of the third photolithography step.

4.4.3 Patterning of backside and release of cantilever

The fourth photolithography was performed to define the membrane at the backside (Fig. 4.16). Again, the backside pattern was aligned to the front side structure already formed in device layer using front-to-back alignment marks. Then a window with corner compensation structures was plasma etched in silicon nitride films at the backside of the wafer.

Before we proceeded with the structuring of backside, the structure at the front side need to be covered with PR5040 as discussed. A thin layer of Allresist AR 300-80 adhesion promoter was applied first by spin coating at 4000 rpm and 2000 $1/s^2$ for 40 seconds and a following baking at 180°C for 2 minutes. This prevents the polymer coating to detach during the long etch process. PR5040 was also spin-coated onto the front side of the sample at 1000 rpm and 2000 $1/s^2$ for 60 seconds. The polymer hardened after a 90 seconds baking at 140°C on the hot plate. The sample is now ready for backside etching.

A deep, anisotropic silicon etching was done in hot 22% KOH solution leaving only 1 µm thick oxide membrane in the future beam area. The wet etching was performed at 70°C with constant stirring at 150 rpm to prevent forming of hydrogen bubbles at sample surface and to ensure that the silicon get supplied with reactants continuously. The etch duration was about 9 hours. It is critical to terminate the etch process at the right time in order to achieve devices with no under- or over-etch because either of those could potentially have a negative effect on the functionality of the device. After the etching the

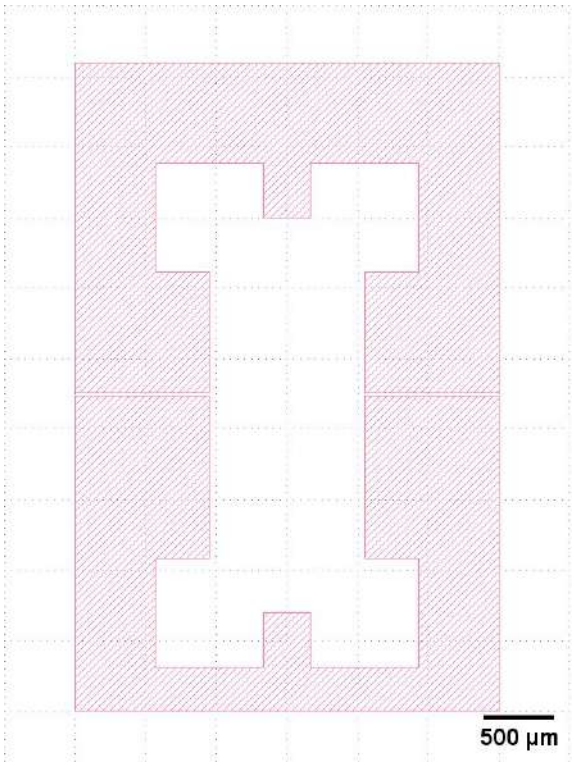


Figure 4.16: Photomask pattern of the forth photolithography step.

sample was dipped into a diluted HCl solution for 2 minutes to remove the metal ions, which are byproducts of the KOH production.

Finally, in the last step, the BOX layer was plasma etched from the backside also with CHF_3 using the standard recipe for 21 minutes to release the cantilever and the protective coating was removed using high power oxygen ashing for 5 minutes. After this step, a free-standing beam was achieved. It has to be cut-off from the chip and wire bonded to the chip-carrier or PCB for testing and measurements.

4.5 Tips on fabrication and improvements

In the earlier fabrication batches, it was realized that the sample surface was usually contaminated after RIE-etching, as shown in Figure 4.17a. This was probably due to contamination of the etch chamber from previous usage of the system. This can be prevented by performing a chamber clean using high power oxygen etching for more than 10 minutes before each actual etch run (Fig. 4.17b). This also applies for the two-step etching of the device layer, the chamber should be cleaned before as well as after the first silicon nitride etch. Another source of contamination on the sample was photoresist residuals especially those after a plasma etch run (Fig. 4.17c). This can be very hard to remove even when using sonication in acetone bath. So to ensure that the resist residuals

won't affect the subsequent fabrication steps, they need to be cleaned thoroughly. A gentle oxygen ashing has proven to be a quick and effective solution (Fig. 4.17d).

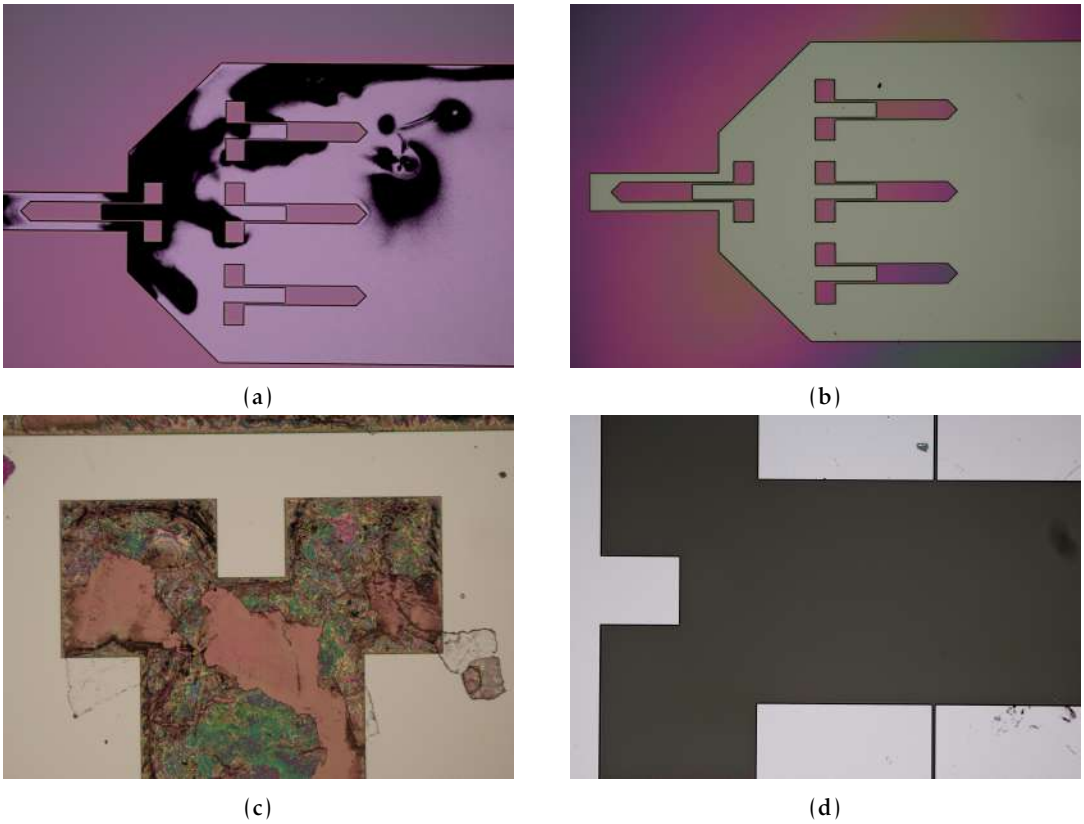
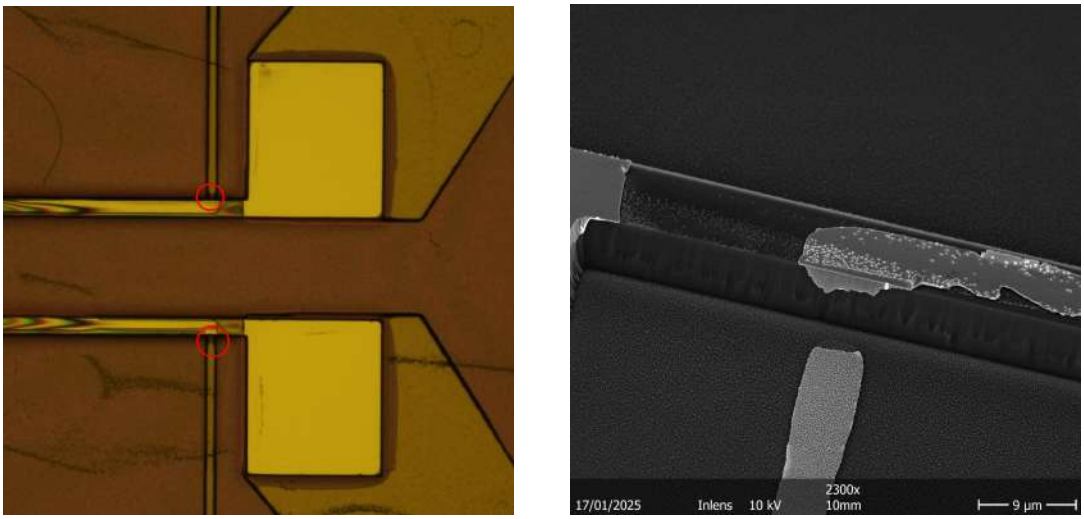


Figure 4.17: Microscope images of the sample after dry etching of front side (**a**) without chamber cleaning, (**b**) with chamber cleaning. And resist residuals on sample surface (**c**) prior oxygen cleaning, (**d**) after oxygen cleaning.

Another problem arises when the electrical contacts are formed. During lift-off, at the transition from chip level to cantilever level, disruptions in the electrical path might happen as shown in the SEM image (Fig. 4.18b). This wouldn't be a problem for sensing function of the cantilever but make it unsuitable for QTM experiments. The reason behind this problems is inhomogeneity spin-coated photoresist on patterned substrate. The resist tends to accumulate in the area when there is a height difference. This can be observed in the microscope image of the sample after spin-coating in Figure 4.18a: the area in proximity of the cantilever appeared darker suggests a thicker resist layer. Knowing the cause of the problem, we tried to modify the lithography step, e.g. a higher exposure dose and/or a longer development duration. This method indeed was improve the situation but not completely solve the problem, as it didn't works hundred percent of the time. Thus we should further improve the recipe or try alternate method of depositing the metal to ensure reliable electrical contacts.

It is also advisable to reduce or to turn-off the stirring completely in the last 30 minutes, since the membrane is very fragile and could potentially break. One could also decide



(**a**) (**b**)

Figure 4.18: (**a**) Microscope image showing resist accumulated near cantilever legs (red circles). (**b**) SEM image of the disruption in electrical path.

whether to terminate the etch process by simply observing the sample. If there is only hydrogen bubbles coming out at four corners means the handle layer was etched through completely and the etch process can be stopped.

One major hurdle that reduced the number of usable cantilevers was the difficulty of separating them from the wafer without damage. In the following, we share the procedure that, based on our experience, proved to be the most effective. It is worth noting that this step may become unnecessary once cantilever production is scaled up.

The first step involves breaking the thin silicon membrane surrounding the cantilever using a fine needle, such as one from a probe station. This step must be performed with great care to avoid damaging the cantilever. At this stage, the cantilever remains attached to the wafer via two small silicon tabs from the handle layer. Next, the sample is cleaved near one of the tabs using a diamond scribe, as illustrated in Figure 4.19. The second tab is then gently scored to weaken it. After scoring, the cantilever can be carefully detached using tweezers.

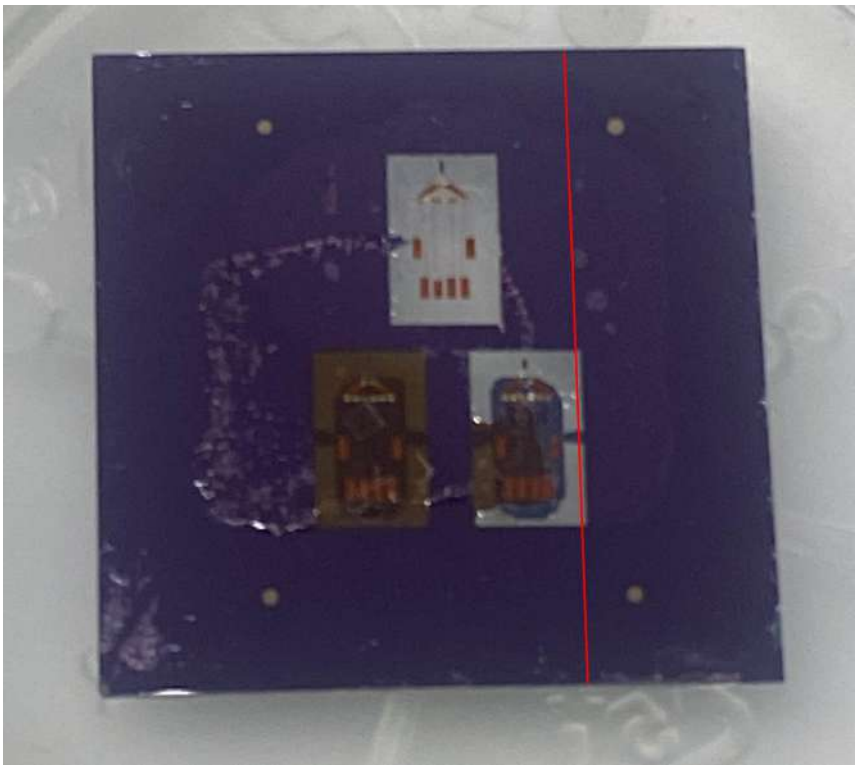


Figure 4.19: Tip on detachment of the cantilever from the chip, red line indicates the cleaving line.

4.6 Characterization of the cantilevers

The successfully fabricated cantilevers were characterized and tested to evaluate their sensing functionality. This section presents and discusses the results of these experiments.

4.6.1 Geometrical properties

As discussed in Chapters 2 & 3, the device geometry has a significant impact on the sensitivity of the cantilevers, particularly the leg length and width, which may vary between fabrication runs. Therefore, to evaluate the consistency and accuracy of the fabrication process, it is essential to measure the actual dimensions of the fabricated cantilevers. This was carried out by inspecting the cantilevers under an optical microscope. The measured dimensions is summarized in Table 4.1.

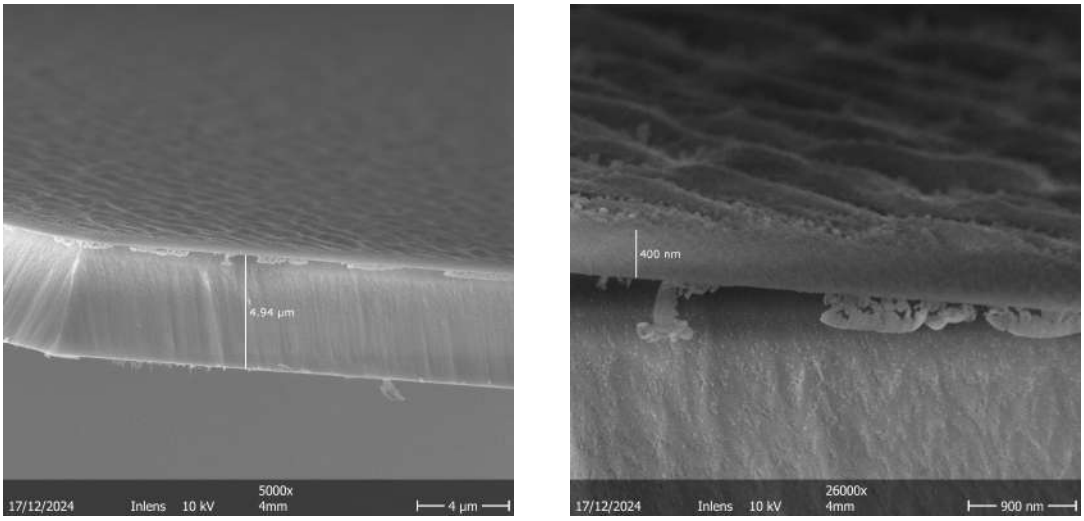
The measured results reveal noticeable variations in both leg length and width between cantilevers and across fabrication runs. When compared with the design values—100 µm for leg length and 15 µm for leg width—it becomes evident that the fabricated structures generally exhibit shorter legs and narrower widths. The reduction in leg length is most prominent in sample s13, where several cantilevers deviate by more than 30 µm from the intended length, likely due to backside mask misalignment. But considering the limited front-to-back alignment accuracy, which was constrained to within 40 µm using the 3D-

Sample	Left leg length	Right leg length	Left leg width	Right leg width
s11	86.65	101.35	12.88	12.40
	87.45	71.94	12.56	12.88
	62.81	88.66	11.61	12.88
s12	88.15	92.95	13.79	13.44
	93.82	93.39	13.61	12.04
	89.02	89.03	13.44	13.79
s13	68.76	68.36	12.32	11.53
	65.18	64.78	11.13	12.32

Table 4.1: Summary of measured cantilever leg width and length.

printed mask method (see Section 4.3.1), this results was acceptable. The narrowing of leg widths, especially in samples s11 and s13, may result from undercutting of the dry etching process. Additionally, the observed asymmetry between the left and right legs, up to 25–30 µm in some cases, can be probably attributed to misalignment with the crystal orientation.

The thickness of silicon and silicon nitride layers were also measured with SEM for only few samples. As shown in Figure 4.20, these parameters were very close to the design, showing no sign of overetching.



(**a**) (**b**)

Figure 4.20: SEM image of the fabricated cantilever showing thickness of (**a**) silicon and (**b**) silicon nitride layer.

These dimensional variations are critical because the cantilever's mechanical and piezoresistive responses depend nonlinearly on the geometry. Specifically, the spring constant scales inversely with the cube of leg length, and even modest reductions can significantly increase stiffness, thereby reducing deflection under applied loads. Similarly,

a narrower leg width increases resistance and could potentially enhance sensitivity but also makes the device more fragile.

Despite these deviations, the consistency in later fabrication runs suggests gradual improvement in process repeatability and alignment precision. Further refinements, such as optimizing the etch duration and exploring more accurate alignment methods, could help bring the fabricated dimensions closer to the design targets and improve inter-device uniformity.

4.6.2 Electrical properties

In order to use the piezoresistive cantilevers for sensing applications, it is important to thoroughly characterize their electrical properties. For this purpose, we measured the current–voltage ($I-V$) characteristics of each element in the integrated Wheatstone bridge, which consists of one active sensing resistor and three reference resistors. Figure 4.21 shows the measurement of one representative device (s11).

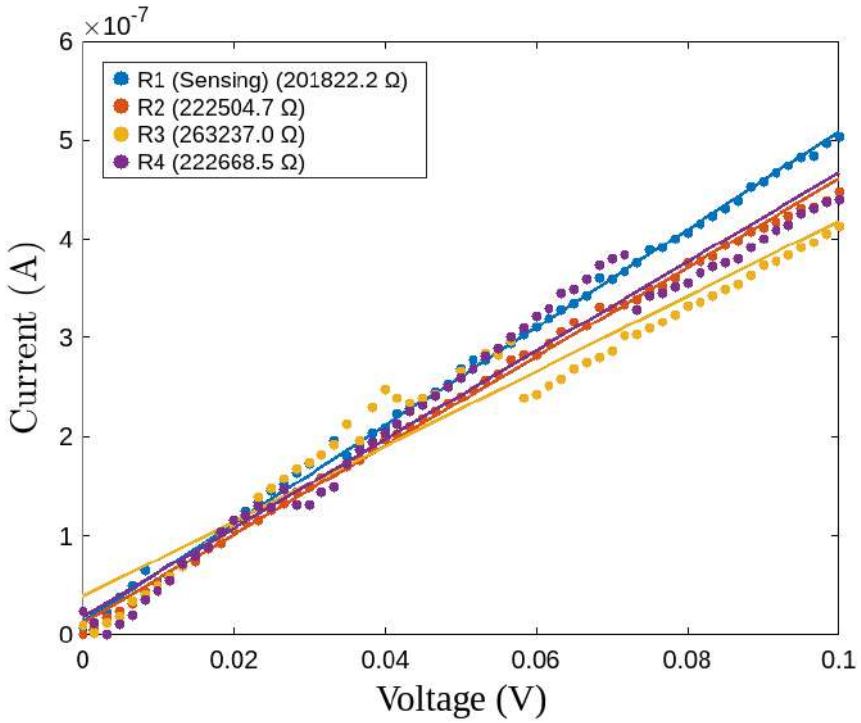


Figure 4.21: Measured $I-V$ curve characteristics of the sensing piezoresitor (R1) and three reference resistors. The solid lines display fitted results to the measurements.

The $I-V$ curves displayed a highly linear behavior, indicating good ohmic contact. Linear fits were applied to extract the resistance values. The calculated resistances of the four elements in the Wheatstone bridge also show noticeable deviations, which may influence the electrical balance and sensitivity of the device. Ideally, all four resistors would be closely matched, especially the three reference resistors, to ensure a minimal

offset voltage in the absence of mechanical stress. In this case, however, the resistors exhibit up to ~10% variation relative to each other. The sensing resistor is approximately 10% lower than the average of the reference resistors. These differences are likely stem from fabrication-related issues such as local variations in etching process. This imbalance within the bridge is particularly important because it may result in an output voltage even when no strain is applied, effectively introducing an offset that needs to be calibrated.

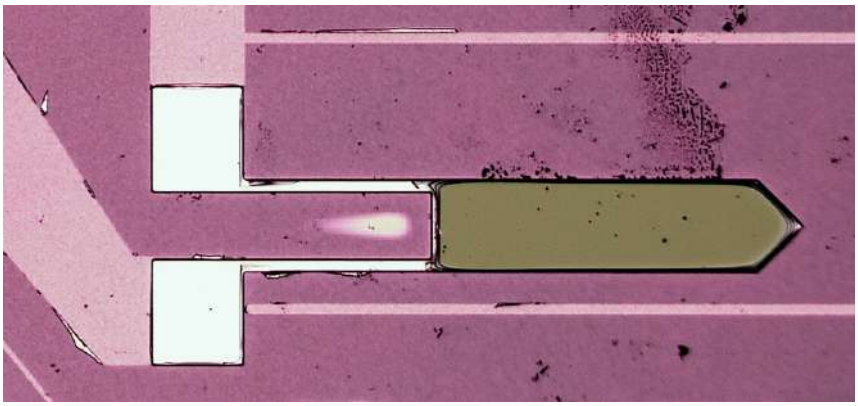


Figure 4.22: Metal residual after lift-off causing shorting in the circuit.

The measured resistances are summarized in the Table 4.2. When compared with the simulated design expectation of approximately 160 kΩ, the measurements show a moderate spread around this value. While most measurements showed higher resistance at around 200 kΩ, some measurements showed lower resistances than predicted value. This deviation can be primarily attributed to fabrication flaws during the lift-off process. In particular, residual gold films were occasionally left bridging across the cantilever legs. As discussed in Section 4.4.2, this occurred especially when the device layer was unintentionally exposed after the dry etching (Fig. 4.14b). These metallic residues effectively created parasitic conductive paths, reducing the overall resistance of the resistors. In the most severe cases, these residues caused complete electrical shorting of the Wheatstone elements (Fig. 4.22). Such instances are reflected in the absence of some data entries in Table 4.2.

Sample	R1 [Ω]	Average (R2-R4) [Ω]	Std Dev [Ω]
s11	573656.8	277340.3	21502.8
	201822.2	236136.7	23469.7
	191539.5	155555	54741.2
s12	242262.5	292545.1	-
s13	192489.6	195537	49355.1
	89049.7	527622.4	32234.3
	148547.4	177844.6	46777.5

Table 4.2: Summary of measured total resistances of fabricated cantilever devices.

The data also show a wide variation in measured resistance values between fabrication runs. For instance, R1 varied from ~89 kΩ to over 570 kΩ, indicating significant inconsistency. Given that these devices were fabricated in an university cleanroom, where fabrication conditions are not as tightly controlled as in the industry, the observed spread in resistance values is understandable. Nonetheless, for the reliable production of cantilevers intended for use in QTM experiments, further refinement of the fabrication process is essential.

Figure 4.23: Schematic illustration of the QTM setup used to deflect the cantilever beam.

4.6.3 Engagement test

To evaluate the sensing functionality of the fabricated microcantilevers, the building test setup for QTM experiments was used (Fig. 4.23). The cantilever chip was wire-bonded to a PCB, which was subsequently mounted into the test setup and positioned using a stack of piezoelectric motors. Since the cantilever did not feature a probing tip, mechanical deflection was induced by pressing it against the edge of a silicon or quartz substrate. A supply voltage of 1.2 V was applied to the Wheatstone bridge circuit, and the resulting output voltage was measured using a Keithley digital multimeter. The signal was recorded during the engagement, with a microscope used to visually confirm the contact between the cantilever beam and the substrate. Only two cantilevers from sample s13 were successfully tested; the remaining devices were damaged during handling or wire-bonding process. Figure 4.24 displays the change in output voltage of the cantilevers during the engagement.

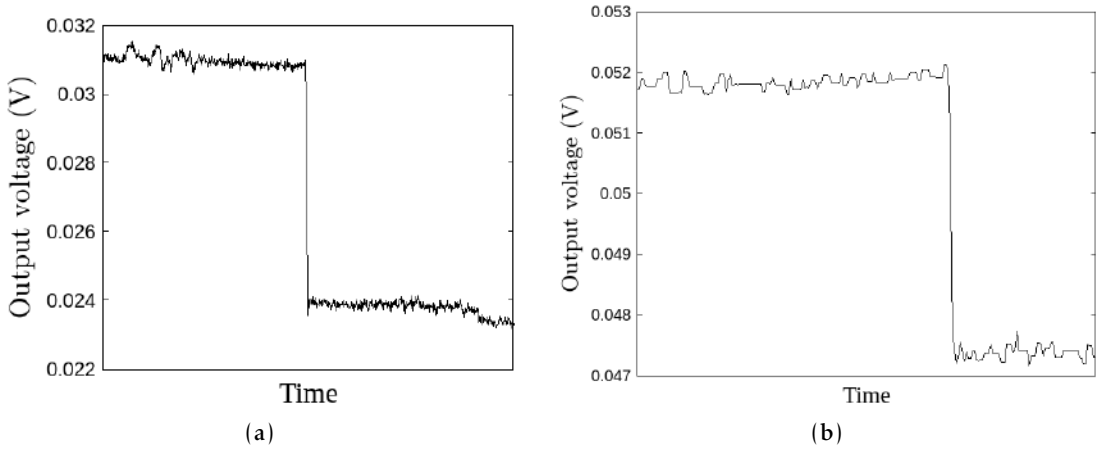


Figure 4.24: Measured output signal of two cantilevers from sample s13.

A pronounced dip of approximately respectively 5 and 7 µV in the output voltage were observed for both tested devices upon contact with the test substrate. In our current setup, no low-noise amplification or filtering was employed, and the measurement was carried out using a standard digital multimeter. Under these conditions, the detected signal was still distinguishable from the background noise. Although it was not possible to quantify the sensitivity of the fabricated cantilevers due to the lack of calibration of the piezomotor system, this simple test clearly demonstrated the functionality of our first cantilever prototype. The observed signal change confirms that the piezoresistive element responds to mechanical deflection, validating the core sensing principle of the device.

5 Conclusions and Outlook

This thesis presented the development of a piezoresistive cantilever intended for application in cryogenic Quantum Twisting Microscope experiments. The primary objective was to design a sensor that is not only compatible with low-temperature operation but also realizable through a fabrication sequence that is both simple and robust. To achieve this, a combination of finite element simulations and process-driven design decisions guided the cantilever development from concept to implementation.

The simulation studies provided valuable insights into how geometrical parameters influence piezoresistive sensitivity. A 3D COMSOL model was developed to analyze the fractional resistance change under load, and the results were used to optimize the cantilever design. It was shown that decreasing the width and thickness of the piezoresistor enhances the output signal. Special care was taken to ensure that the final geometry remained within fabrication feasibility while still delivering adequate sensitivity.

Beside simulation, considerable effort was made to the fabrication of the cantilevers. Key challenges such as backside alignment and etching-related complications were identified and addressed in the process design. Simple cleanroom recipe was established using SOI wafers as starting point that enables a relatively reliable fabrication of piezoresistive cantilevers. It has been demonstrated that the fabricated cantilevers are fully functional at room temperature. Although the final devices are yet to be integrated and tested at cryogenic temperatures, the groundwork in this thesis provides a good foundation.

While the fabricated piezoresistive cantilevers have demonstrated promising performance, there remains considerable room for further improvements. One notable constraint in the current fabrication process is the front-to-back alignment. It was observed that features etched from the backside could be identified from the front, suggesting a potential method for more accurate alignment using etched markers. This approach was not pursued further in this thesis due to its additional complexity. However, future work could address this by scaling up the fabrication process. By performing the fabrication on full wafers rather than individual chips, alignment markers could be etched for the entire wafer in a dedicated step, enabling more accurate and efficient alignment for all subsequent lithography processes. The choice of substrate also presents limitations. The use of a standard SOI wafer offered a straightforward process flow, but it constrained both the thickness of the cantilever and the piezoresistive layer. Exploring alternative methods, such as local doping via spin-on-dopants or focused ion beam implantation, could significantly improve the design flexibility. Furthermore, future work should be directed more toward the end goal, which is employing the cantilever in low temperature QTM experiments. As first step, compatibility of fabricated cantilevers could be tested in room-temperature QTM setups. Critical next milestone is the operation and characterization of these cantilevers at cryogenic temperatures. The current doping level of the SOI wafer may be insufficient at low temperatures, where carrier freeze-out becomes relevant. Investigating substrates with higher doping concentrations therefore would be an apparent next step to ensure robust performance under cryogenic conditions.

List of Figures

List of Tables

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Erklärung zur Masterarbeit

Declaration Master Thesis

Ich versichere, dass ich die Arbeit selbstständig angefertigt, nicht anderweitig für Prüfungszwecke vorgelegt, alle benutzten Quellen und Hilfsmittel angegeben, sowie wörtliche und sinngemäße Zitate gekennzeichnet habe.

I declare that this thesis has been composed by myself, and describes my own work, unless otherwise acknowledged in the text

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